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Chapter 5: Design and Characterization of Wide-Tuning CMOS Active Inductors for RF and Microwave Applications

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Abstract: This chapter presents the design, implementation, and evaluation of a tunable active inductor implemented in standard 130 nm CMOS technology. Two topologies are proposed: a single-ended implementation based on an enhanced cascode-grounded gyrator-C structure, and a differential topology incorporating negative-resistance compensation. In this design, independent inductance/quality factor (Q) tuning is achieved in the single-ended circuit through a dual control mechanism represented by the feedback resistor and bias currents, while the differential topology expands this concept to take advantage of cross-coupled devices for loss cancellation, offering enhanced Q and wide inductance tunability. The two structures were fabricated and measured, and both post-layout simulated and measured results exhibit compact silicon area, wide frequency tunability, excellent Q-factor performance, and low noise figures. The proposed tunable active inductors feature great robustness to PVT variations and are ideally suitable for integration into RF building blocks including filters, oscillators, and low-noise amplifiers.

Keywords: Tunable Active Inductor, Gyrator-C Topology, CMOS Implementation, High-Q, RF Integrated Circuit, Wide Tuning Range,

1 Introduction

The integration of high-performance inductive elements remains an open challenge in RF and microwave circuit design. Though on-chip passive inductors, which present limited quality factor, large area occupation, and poor tunability, active inductors ensure compactness and flexibility. Various approaches were developed for the implementation of active inductors, and among them, the gyrator-C-based configurations have attracted significant attention due to their capabilities of emulating large inductance values with electronic tunability of both inductance and quality factor (Behera et al., 2022).

Recent research has focused on improving active inductor performance through enhanced topologies, more sophisticated biasing schemes, and compensation for intrinsic losses. However, practical designs need also to satisfy other key constraints, including compact layout, wide tuning range, low noise, and robustness to process variations (Patel et al., 2018).

This chapter presents two improved CMOS tunable active inductors to meet the above demands. The first one is a single-ended cascode-grounded topology where inductance and Q are tunable independently with an active feedback resistance and controlled current sources. The second one is a differential version obtained by combining two single-ended cells with cross-coupled negative-resistance devices boosting Q and extending the tuning range. Both topologies are fabricated in a 130 nm CMOS process and verified with post-layout simulations and measurements.

The chapter is organized as follows: In Sect. 2, single-ended topology and its tuning mechanisms are described. Then, in Sect. 3, the differential version and enhancements are presented. Sections 4 and 5 report simulation and measurement results about inductance/Q tuning, noise, linearity, and robustness under PVT variations. Finally, the main advantages and integration potential of the proposed designs are discussed in this chapter.

2 Design of an Enhanced Tunable Active Inductor: The Single-End Version

2.1 Topology Description

A simplified schematic of the TAI is shown in Fig. 5.1, from (Hammadi et al. 2014; Hammadi et al. 2017). The structure is inspired from a cascode-grounded topology described in (Thanachayanont et al. 1996), which has been widely adopted due to its ability to increase the inductance value and enhance the quality factor. The realization of the proposed structure offers the proper degrees of freedom to allow independent tuning of the inductance value and the quality factor. The two main mechanisms adopted to perform the tuning are: (i) the addition of a feedback resistance, and (ii) the use of controlled current sources. The combination of such elements greatly increases the tuning range of the equivalent inductance, L, and the quality factor, Q.

The insertion of transistor M3, stacked over M1, effectively decreases the equivalent output conductance g_{ds1}. This evidently reduces the series resistance and increases the effective inductance considerably, which also agrees with the analysis in Ref. (Thanachayanont, 2002).

Additional enhancement is carried out by adding an active feedback resistance, implemented via transistor M4, between M2 and M3. The added element presents an additional inductive reactance at the source terminal of M2, further increasing the equivalent inductance of the cascode-grounded structure. This directly translates into a higher quality factor for the circuit.

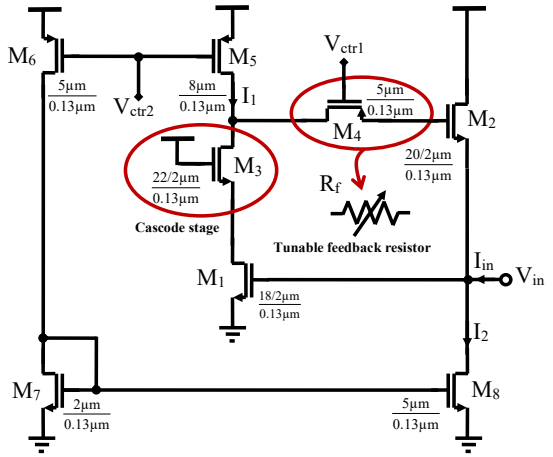


Fig. 5.1 Simplified schematic of the proposed single-ended active inductor.

The biasing current sources I1 and I2 are realized with transistors pairs (M7-M8) and (M5-M6), respectively. Assuming ideal current sources, the small-signal equivalent model of the proposed single-ended version AI is shown in Fig. 5.2.

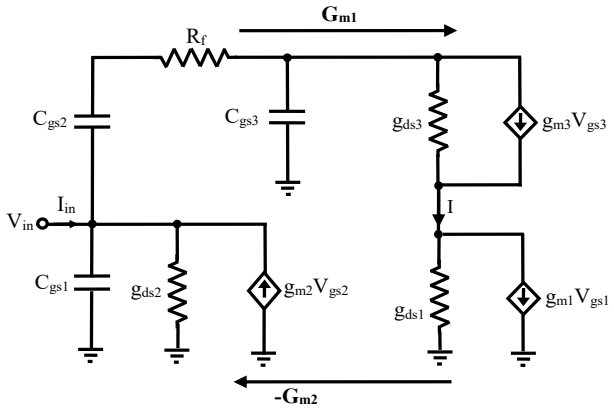


Fig. 5.2 Small-signal equivalent circuit of the single-ended active inductor.

The equivalent parameters of the proposed active inductor, namely, the parallel capacitance, C_p, parallel resistance, R_p, series resistance, R_s, and effective inductance, L_s are derived and given in Equations 102–104. Note that for tractability, some higher order parasitic effects including the finite output impedance of the transistors and the gate–drain capacitance, C_{gd} have been neglected in the small-signal analysis.

$$L_s = \frac{C_{gs2} g_{m2} g_{m3} + \omega^2 C_{gs2}^2 C_{gs3} \left(1 + g_{ds3} R_f\right)}{g_{m1} g_{m3} g_{m2}^2 + \omega^2 C_{gs2}^2 g_{m1} g_{m3}} \tag{102}$$

$$R_s = \frac{g_{ds1} g_{ds3} g_{m2} + \omega^2 \left(C_{gs2}^2 g_{m3} - C_{gs2} C_{gs3} g_{m2} \left(1 + g_{ds3} R_f\right)\right)}{g_{m1} g_{m3} g_{m2}^2 + \omega^2 C_{gs2}^2 g_{m1} g_{m3}} \tag{103}$$

$$R_p = \frac{1 + g_{ds3} R_f}{g_{ds3} \left(2 + g_{ds3} R_f\right)} \tag{104}$$

$$C_p = C_{gs1} \tag{105}$$

Assuming $g_{m2}^2 >> \omega^2 C_{gs2}^2$, equivalent inductance can be approximated to be:

$$L_s = \frac{C_{gs2} g_{m2} g_{m3} + \omega^2 C_{gs2}^2 C_{gs3} \left(1 + g_{ds3} R_f\right)}{g_{m1} g_{m3} g_{m2}^2} \tag{106}$$

where g_{ds1}, g_{ds2}, g_{ds3} are the output conductances of transistors M1, M2, and M3, respectively, while C_{gs1}, C_{gs2}, C_{gs3} are the corresponding gate–source capacitances at nodes 1, 2, and 3, respectively. Also g_{m1}, g_{m2}, g_{m3} represent the transconductances of M1, M2, and M3, respectively.

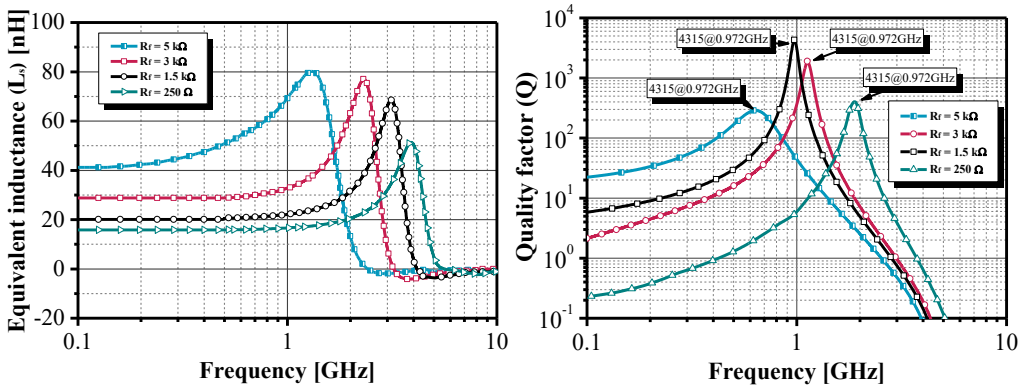
This formulation emphasizes how heavily L_s depends on the intrinsic transistor parameters as well as on the feedback mechanism of the circuit. In particular, the cascode transistor M3 plays a very important role: by suppressing the effect of g_{ds1}, L_s is increased and the quality factor enhanced.

2.2 Inductance and Q Tuning Methods

As discussed before, the single-ended TAI supports multiple degrees of freedom for tuning its effective inductance and quality factor. Two complementary tuning techniques are employed in this design.

(i) Feedback-resistance tuning: As shown in Equation (106), changing the feedback resistance R_f directly alters the equivalent input reactance and thus affects the extracted inductance and resonance frequency. Fig. 5.3 shows that when R_f is swept from 250 Ω to 5 kΩ, the inductance varies from approximately 5.17 nH to 8.02 nH, while the resonance frequency shifts from around 1.3 GHz to 3.88 GHz. To achieve a compact and low-noise implementation compatible with the cascode-grounded structure, R_f is realized using a PMOS transistor operating in the linear region and controlled by the gate voltage V_{ctr1}. Using a PMOS "active resistor" offers two practical benefits: (a) better noise performance than an NMOS device in this biasing condition, and (b) isolation

through dedicated n-wells, which reduces body-effect nonlinearity. Consequently, varying V_{ctr1} adjusts the small-signal conductance of M4, enabling smooth, monotonic tuning of the equivalent feedback resistance.



(a) (b)

Fig. 5.3 Tuning characteristics of (a) equivalent inductance and (b) quality factor with respect to the feedback resistor R_f.

(ii) Bias-current tuning: The second tuning control is provided by the bias network. In this design, the current source I2 is implemented with a voltage-controlled transistor, and adjusting the control voltage V_{ctr2} jointly drives I1 and I2. This co-variation modifies the transconductances g_{m1}, g_{m2}, and g_{m3} (see Table 5.1), thereby tuning both the equivalent inductance Ls and the quality factor Q simultaneously, following Equations (107–109):

$$\omega_z = \frac{g_{ds1}g_{ds3}g_{m2} + \omega^2\left(C_{gs2}^2 g_{m3} - C_{gs2}C_{gs3}g_{m2}\left(1+g_{ds3}R_f\right)\right)}{C_{gs2}g_{m2}g_{m3} + \omega^2\left(C_{gs2}^2 C_{gs3}\left(1+g_{ds3}R_f\right)\right)} \tag{107}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m3}g_{m2}^2 + \omega^2 C_{gs2}^2 g_{m1}g_{m3}}{C_{gs1}C_{gs2}g_{m2}g_{m3} + \omega^2\left(C_{gs2}^2 C_{gs1}C_{gs3}\left(1+g_{ds3}R_f\right)\right)}} \tag{108}$$

$$Q = \frac{C_{gs2}g_{m2}g_{m3}\omega + \omega^3 C_{gs2}^2 C_{gs3}(R_f g_{ds3}+1)}{g_{ds1}g_{ds3}g_{m2} + \omega^2(C_{gs2}^2 g_{m3} - C_{gs2}C_{gs3}g_{m2}(R_f g_{ds3}+1))} \tag{109}$$

Bias-current tuning is particularly effective for coarse adjustment of the operating band (through gm-dependent poles and zeros), while R_f tuning allows for fine control of Q and the inductive slope.

In practice, these two controls operate hierarchically: V_{ctr2} determines the target frequency range and inductance window by setting the gm levels, and then Vctr1 fine-tunes R_f to optimize Q and compensate residual series losses without significantly

disturbing L. This hierarchical control scheme improves post-layout calibration convergence and helps preserve linearity by preventing large variations in either control.

Table 5.1 Tuning characteristics of transconductances under varying current source levels.

I_1 [µA]	I_2 [µA]	g_{m1} [mS]	g_{m2} [mS]	g_{m3} [mS]
10	80	16.6	0.1	0.2
100	80	18.6	1.8	1.9
150	100	18.8	2.6	2.6
200	10	18.9	3.2	3.3
200	50	19.0	3.2	3.3
200	80	18.6	3.2	3.3

3 Design of an Enhanced Tunable Active Inductor: The Differential Version

The differential active inductor (DAI) proposed in this work, shown in Fig. 5.4 (Hammadi et al., 2015; Hammadi et al., 2016), is a symmetrical circuit made up of two cascode-configured gyrator-C tunable active inductors. The NMOS transistors M1, M2, M9, and M10 form the core inductive structure. When a differential input signal is applied to the gates of the common-source transistors M1 and M9, the respective transconductances (g_{m1} and g_{m9}) convert this voltage into drain currents that charge the gate–source capacitances C_{gs2} and C_{gs10} of transistors M2 and M10. The voltages that appear across these capacitances are then reconverted into input currents through the transconductances of M2 and M10, which effectively reproduce the current–voltage behavior of a shunt inductor.

To improve performance further, transistors M3 and M11 are used as gain-boosting devices to lower the output conductances (g_{ds}) of M1 and M9. This reduction in g_{ds} leads directly to an increase in both the effective inductance and the achievable quality factor. The bias currents for the transistor pairs (M1, M2) and (M9, M10) are provided through the current mirrors M5–M8 and M13–M16, respectively.

The feedback resistors are realized using PMOS devices (M4 and M12) operating in the linear region, while the current sources are implemented with controlled current mirrors. This setup allows for tuning flexibility, compact design, and efficient biasing.

To minimize parasitic resistances and enhance the quality factor in a differential active inductor, a negative resistance technique is commonly used. This negative resistance compensates for the resistive component, thereby improving the overall quality factor (Thanachayanont et al., 2000; Ler et al., 2008). In this design, the negative resistance is created using a pair of cross-coupled transistors connected to the input terminals of the differential active inductor. Transistors M17 and M18 form this negative-resistance

network. Their sizes and bias conditions are carefully selected to achieve the desired transconductance at the inductor's operating current. Besides defining the transconductance, these devices contribute to maintaining a high quality factor by generating a negative conductance that offsets the intrinsic losses of the active inductor.

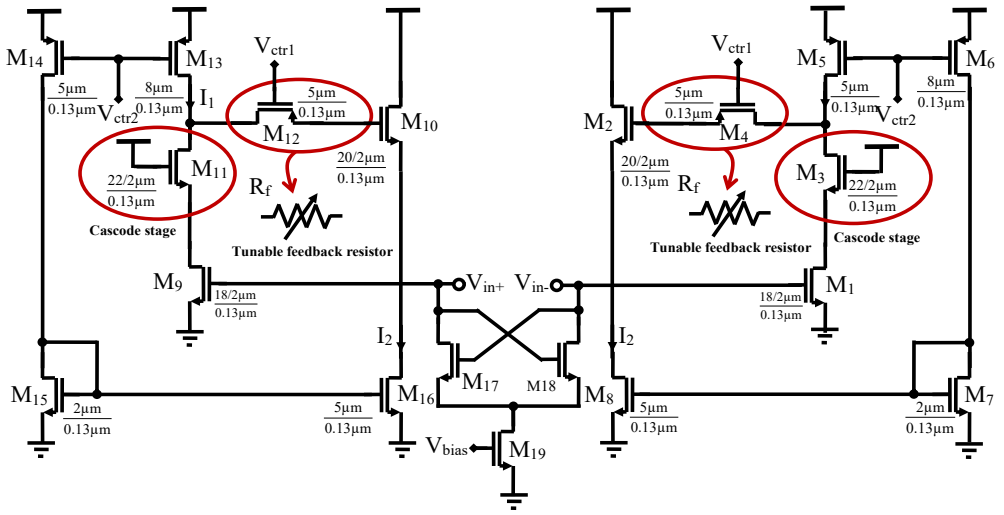


Fig. 5.4 Simplified schematic of the proposed single-ended active inductor.

Through this mechanism, the loss mechanisms inherent to a differential active inductor can be substantially mitigated. The resulting equivalent inductance and Q-factor can be expressed as:

$$L=\frac{2\left(\omega^2 C_{gs1}^2 C_{gs2}\left(1+\frac{g_{ds1}}{g_{ds4}}\right)+g_{m1}g_{m2}C_{gs1}\right)}{\left(\omega^2 C_{gs1}^2 g_{m2}g_{m3}+g_{m1}^2 g_{m2}g_{m3}\right)g_{m18}} \tag{110}$$

$$Q=\frac{\omega\left(C_{gs3}\left(1+\frac{g_{ds3}}{g_{ds4}}\right)\omega^2 C_{gs2}^2+g_{m2}g_{m3}C_{gs2}\right)}{\omega^2\left(C_{gs1}^2 g_{m3}-C_{gs2}C_{gs3}g_{m2}\left(1+\frac{g_{ds3}}{g_{ds4}}\right)+g_{ds1}g_{ds3}g_{m2}\right)g_{m18}} \tag{111}$$

The novelty in this design is the method of adjusting the inductance, which is realized by concurrently tuning the active feedback resistor and the bias current sources. The resistance value of the feedback network is controlled by the gate voltage V_{ctr1}, while the variation of the current sources is controlled by the control voltage V_{ctr2}.

4 Results of the Single-Ended Active Inductor

4.1 Test Setup

As proof of concept, the grounded tunable active inductor was fabricated in 130 nm CMOS technology from STMicroelectronics®. Characterization was carried out under nominal process–voltage–temperature (PVT) conditions and all reported results correspond to this typical corner. A total of 25 chips were tested, showing a narrow distribution of performance metrics, confirming the consistency and reliability of the design under standard operating conditions (Saad et al., 2025). A die photograph of the fabricated circuit is presented in Fig. 5.5, where the total chip area including bond pads is 400 µm×345 µm, while the core active inductor occupies only 25.3 µm×12.2 µm (308.7µm²) without pads.

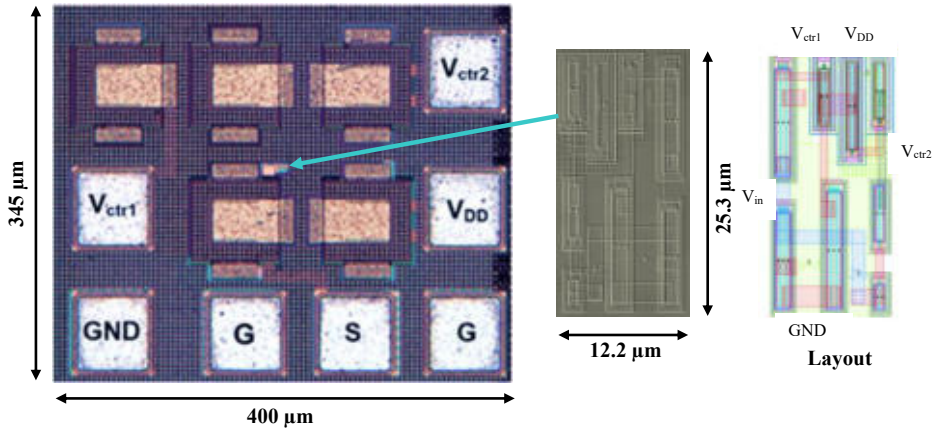


Fig. 5.5 Die micrograph of the fabricated single-ended active inductor (AI).

Fig. 5.6 Test setup: active inductor on top right and the corresponding measurement bench on the left. Unless otherwise mentioned, all performance values reported in the following are deem bedded for the loading effects introduced by the RF input pads.

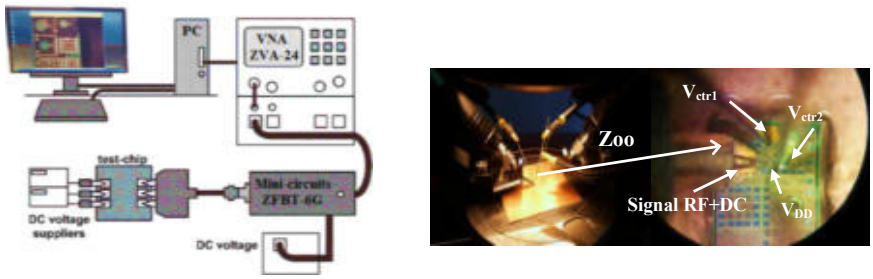


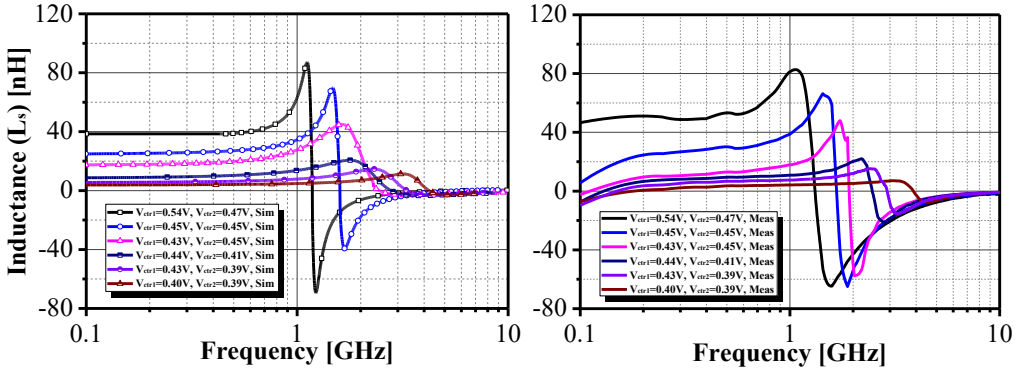
Fig. 5.6 Test setup used for on-wafer RF measurements of the fabricated single-ended AI.

As stated before, this was achieved with 20 pF on chip decoupling capacitors. The on-wafer measurements were carried out by means of a Rohde & Schwarz ZVA-24 vector network analyser (VNA) with the use of appropriate RF and DC probes. All measurements were conducted at a circuit bias voltage of 1V with an input signal amplitude of –20 dBm (27°) at 2 GHz. The power consumption of the grounded active inductor was 2.0 mW, most of which was dissipated in the gyrator-C core.

4.2 Post-Layout and Measurement Results: SRF, Inductance and Q Performances

The performance of the proposed circuit, shown in Fig. 5.1, was first simulated with Spectre RF® from Cadence using a 130 nm CMOS process from STMicroelectronics®. Measurement results, after post-layout extraction, were carefully looked at and compared to post-layout simulation and to state-of-the-art designs present in literature.

From the S-parameter analysis, the inductance and quality factor variation of the tunable active inductor is shown in Fig. 5.7. The tuning mechanism is implemented by properly biasing: the feedback resistance is adjusted through V_{ctr1} between 0.4 and 0.54 V, whereas the current sources are controlled by V_{ctr2}, which varies between 0.39-0.47 V.



(a) (b)

Fig. 5.7 Equivalent inductance response of the single-ended TAI under varying control conditions: (a) Post-layout simulation (b), experimental measures.

Fig. 5.7 shows that the inductance can be tuned over a very wide frequency range: from 668 MHz to 3.96 GHz, which corresponds to an inductance variation from 6.7 nH to 84.4 nH. Fig 5.8 shows the measured quality factor for various configurations of the control voltage. Quality factors as high as 50 are obtained across frequency-independent regions. The maximum quality factor of 1586 was measured at 1.9 GHz for bias voltages of V_{ctr1}=0.43V and V_{ctr2}=0.41V. In general, the measurement results of Fig. 5.7 and Fig. 5.8 confirm the trends reported in Fig. 5.3, and thus confirm the expected behavior.

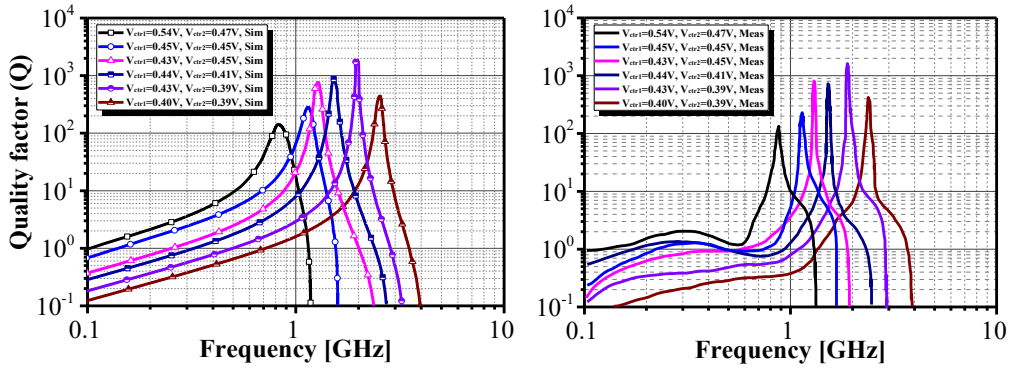


Fig. 5.8 Quality factor response of the single-ended TAI under varying control conditions: (a) Post-layout simulation (b), experimental measures.

Slight deviations between measured and simulated equivalent inductance and quality factor are observed due to parasitic effects introduced by the fabricated layout. In practice, discrepancies of this nature arise through parasitic capacitances and resistances and other layout-dependent issues, as commonly found. The frequency-dependent nature of the transconductor influences the results further, as the transconductance gm drops off with increasing frequency, resulting in variations in impedance transformation and therefore variations in the quality factor as well.

Additional degradation comes through intrinsic parasitic capacitances, specifically the gate–source capacitance, C_{gs}, and gate–drain capacitance, C_{gd}, as well as through the finite output resistance of the transistors. These non-idealities lead to associated energy losses that lower the attainable quality factor over many frequency ranges. Fabrication-related spreads, such as those due to oxide thickness or interconnect dimensions, may also alter effective parasitic capacitances, thereby increasing these effects. In integrated RF circuits, such spreads in the quality factor impact performance directly and result in lower selectivity in bandpass filters, increased insertion loss in matching networks, and higher phase noise in oscillators.

From the measured S-parameters, equivalent inductance and quality factor (Q) were extracted, further confirming the performance of the inductor. Fig. 5.9 presents the equivalent inductance as a function of the control voltages V_{ctrl} and V_{ctr2}, where the supply voltage was kept at V_{DD}=1V. Two measurement conditions were used: the feedback resistance R_f was kept constant and the transistor conductance g_{ds5} was kept constant. As it appears from Fig. 5.9, the equivalent inductance L_s follows a linear tuning profile while the quality factor shows its maximum at around 1.5 GHz and 1.9 GHz.

To investigate the robustness and stability of the proposed active inductor against process and mismatch variations, a Monte Carlo analysis of 100 iterations was carried out as shown in Fig. 5.10.

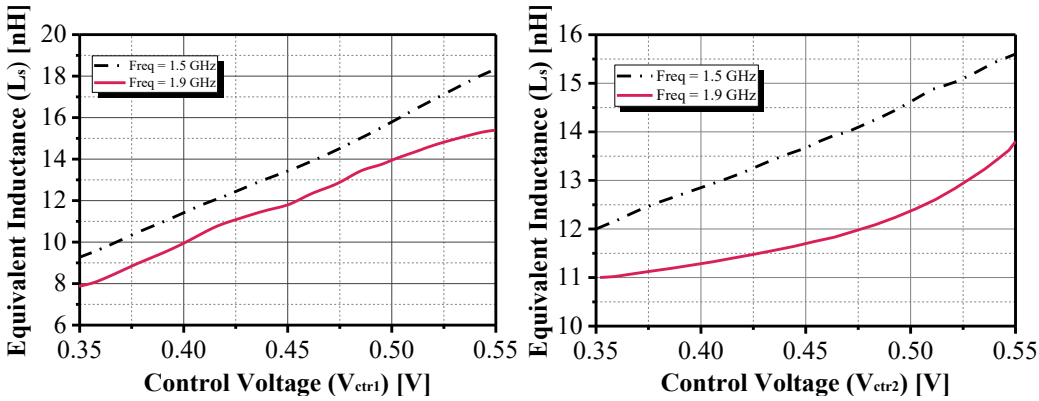


Fig. 5.9 Equivalent inductance and quality factor versus (a) control voltage V_{ctr1} (with g_{ds5} held constant) and (b) control voltage V_{ctr2} (with feedback resistor R_f fixed).

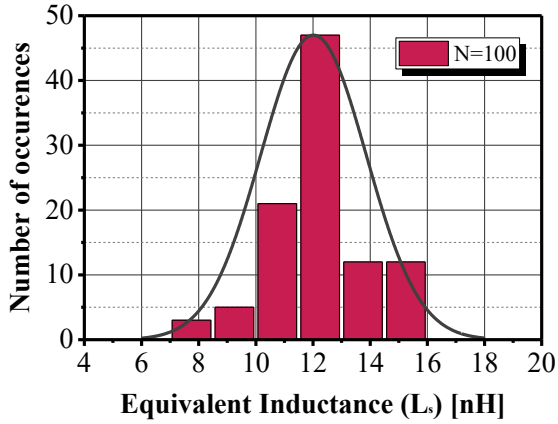


Fig. 5.10 Monte Carlo analysis for the single-ended AI circuit under ±10% mismatch and process variations: post-layout simulations.

In this simulation, ±10% Gaussian distribution was applied to the aspect ratios of the transistors. The results in Fig. 5.10 show that the inductance varies between a minimum of 7 nH and a maximum of 16 nH. It is further noticed that nearly 65% of the samples are between 10 and 13 nH, clustering around the nominal value of the inductance, which is 12.8 nH (i.e., L is selected at the frequency of Q).

4.2 Noise, Linearity and Stability Assessment

Noise characteristics of the proposed tunable active inductor are shown in Fig. 5.11(a). The plot represents the output noise voltage for the control voltages V_{ctr1}=0.4V and V_{ctr2}=0.39 V, corresponding to a resonance frequency of 3.96 GHz. From the results it can be seen that the circuit has less than 2.9 nV/Hz output noise voltage within its tunable range from 0.668 up to 3.96 GHz. When compared to previously reported designs

(Uyanik et al., 2007; Ebrahimzadeh et al., 2011; Rafai et al., 2013), the proposed active inductor features a lower noise profile, suitable for integration in RF building blocks such as low-noise amplifiers, LC oscillators, and active filters.

On the other hand, linearity of the circuit has also been investigated. Here, referring to Fig. 5.11(b), the linearity of the active inductor is defined by its input-referred 1 dB compression point. From the figure, it is observed that the circuit exhibits an input-referred compression point of 5.02 dBm corresponding to an output power of about 6.85 dBm.

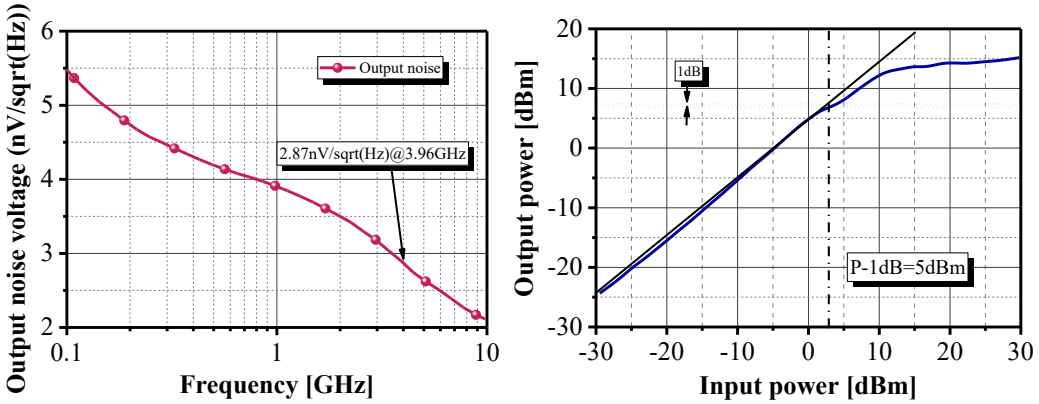
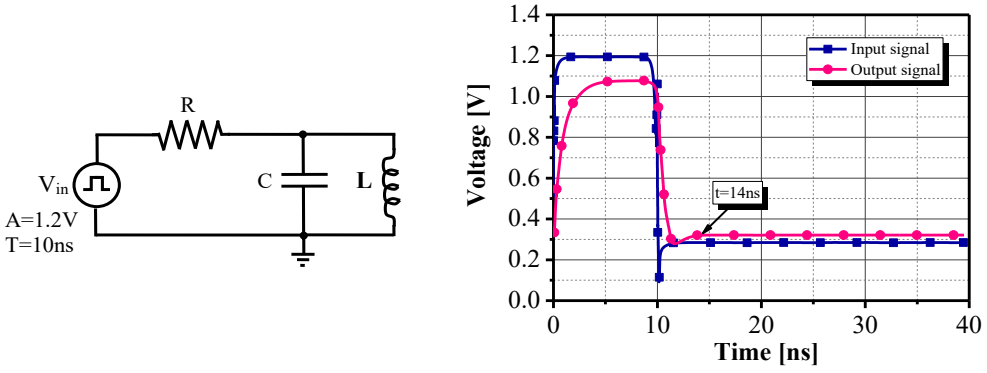


Fig. 5.11 (a) Output noise voltage characteristics, and (b) Input-referred 1-dB compression point of the single-ended AI.

For studying the stability of the SE AI, it was placed in a filtering network as shown in Fig. 5.12(a). Transient analysis was performed with R=1 kΩ presenting a high impedance to the output. The response, depicted in Fig. 5.12(b), reveals that after about 14 ns, the circuit settles to its steady state. Thus, the tunable active inductor possesses good stability properties.



(a) (b)

Fig. 5.12 (a) Stability test circuit, and (b) its corresponding response.

5 Results of the Differential Active Inductor

The proposed tunable differential active inductor has been designed based on a standard 130 nm CMOS process from STMicroelectronics® to validate the operation of the system for a wide frequency tuning range. Post-layout simulations have been realized by using the Spectre RF® simulator in the Cadence® design environment. The layout of the differential active inductor is given in Fig. 5.13, where it shows a symmetrical structure that ensures improved device matching. The core circuit occupies a very compact area of about 430 µm×475 excluding pads as described in (Hammadi et al. 2015; Hammadi et al. 2016).

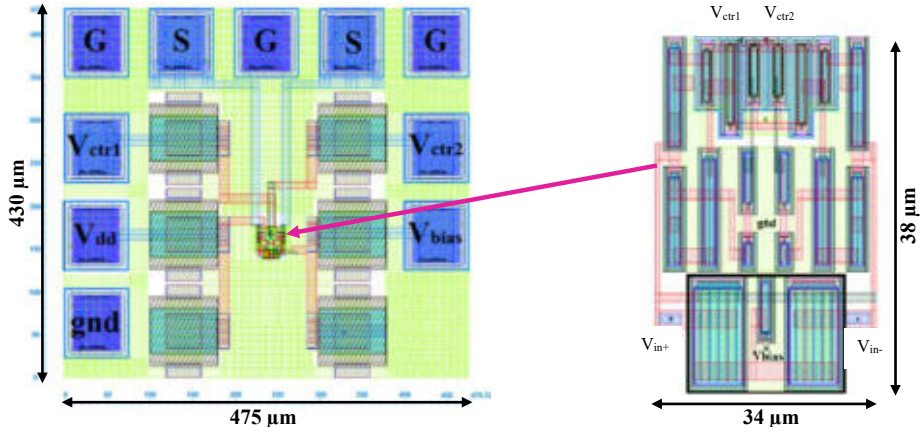


Fig. 5.13 Layout including pads of the differential active inductor (AI).

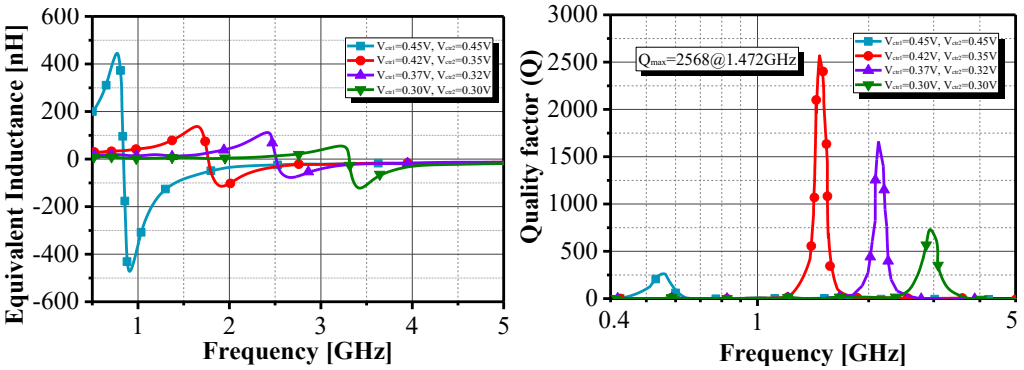
In this layout, the design rule check requirements are satisfied, including short interconnect lengths and having the appropriate metal widths. The parasitic capacitive and resistive effects of the interconnections have been included in the simulations, choosing dimensions to minimize signal losses. A ground plane is used to isolate the substrate interconnections, which allows for more accurate modeling of the overall structure.

This section presents the post-layout simulation results in terms of SRF, inductance variation, and Q-factor tuning. Phase response was also verified to confirm inductive behavior of the circuit. Power dissipation, noise performance, and linearity are some further analyses.

5.1 Post-Layout Simulations: SRF, Inductance and Q Performances

The extracted equivalent resistance, Real(Z_{in}), and reactance, Imag(Z_{in}), of the input impedance Z_{in} determine the quality factor and inductance of the differential active inductor. Fig 5.14(a) shows the characteristics of inductance versus frequency obtained from post-layout simulations for various combinations of V_{ctr1} and V_{ctr2}. With proper

tuning of the feedback resistance and also current sources using the control voltages V_{ctr1} and V_{ctr2}, a wide range inductance tuning can be achieved. More specifically, by varying V_{ctr1} and V_{ctr2} from 0.3 V to 0.45 V, the inductance increases from 19 nH to 440 nH along with an operating frequency range extending from 0.5–3.4 GHz.

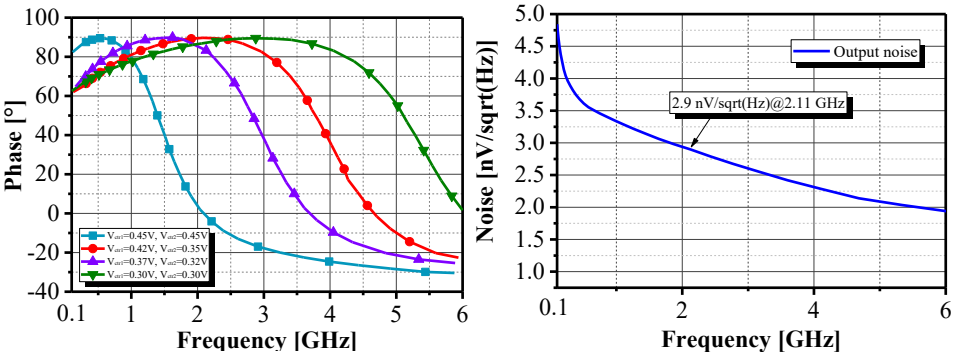


(a) (b)

Fig. 5.14 Post-layout simulated: (a) equivalent inductance, and (b) Q-factor, responses of the proposed DAI versus frequency for various control voltage settings.

Fig 5.14(b) indicates that the quality factor of the proposed DAI is also tunable over a very wide range. Simulation results show that its quality factor varies from about 290 at 0.55 GHz to 730 at 2.93 GHz and goes up to almost 2600 at 1.472 GHz for V_{ctr1}=0.42V and V_{ctr2}=0.35V. An excellent correspondence between schematic-level and post-layout simulation results further verifies the validity of the design. Wide tuning capability of Q represents one of the major advantages of this implementation.

Further verification of the inductive behavior was performed by analyzing the phase response of the DAI. In Fig. 5.15(a), the phase approaches 90° across the operating frequency band, confirming that the circuit maintains inductive characteristics throughout its tuning range.



(a) (b)

Fig. 5.15 (a) Phase characteristics of the input impedance ($\angle Z_{in}$) for the differential AI under different V_{ctr1} and V_{ctr2} settings, and (b) Output noise voltage characteristics.

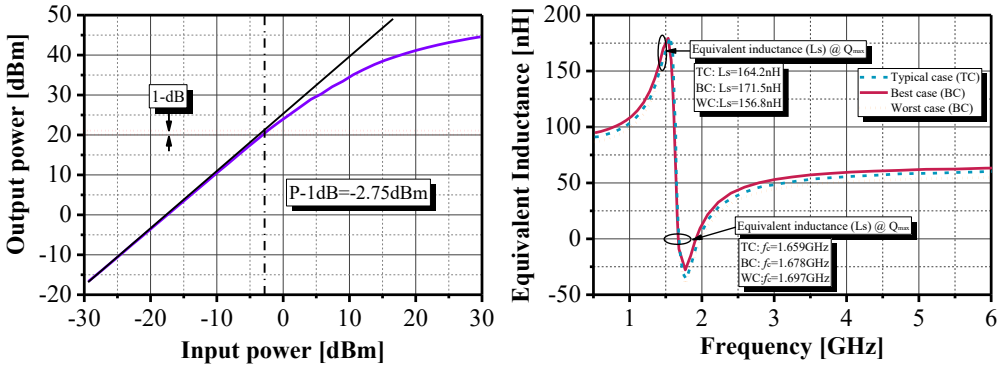
5.2 Noise, Linearity and Corners Analysis

Noise performance of the DAI is also measured and results are shown in Fig. 5.15(b). For a set of control voltages V_{ctr1}=V_{ctr2}=0.45V, that corresponds to a resonance frequency of 2.111 GHz, the circuit exhibits an output noise voltage below 2.9 nV/Hz.

Linearity has been checked by means of the 1 dB compression point whose simulated result is reported in Fig. 5.16(a). The circuit exhibits an input-referred compression point equal to –2.75 dBm that guarantees acceptable linearity for RF applications.

In addition, PVT variations have been analyzed through statistical and corner simulations. The result for a representative bias condition of V_{ctr1}=0.42V and V_{ctr2}=0.35V is shown in Fig. 5.16(b). The worst-case is represented by the worst-case corner (slow–slow process), supply voltage of 0.9 V, and temperature of 125 °C. The best-case corner (fast–fast process) is obtained for a supply of 1.1 V and a temperature of –40 °C whereas the typical case refers to nominal process conditions at 1.0 V and 25 °C.

From these results, the inductance deviations with respect to the typical case were found to be ±4.5%, and in frequency ±0.11% both in the worst and best conditions. These values confirm that the proposed DAI has strong robustness against PVT variations, thus ensuring stable performance over a wide range of operating environments.



(a) (b)

Fig. 5.16 (a) 1-dB power linearity characteristics of the differential AI, and (b) inductance response under process variations (TC, BC, and WC).

Conclusion

This chapter has presented two CMOS tunable active inductor designs that combine compact implementation with high performance: The single-ended version, based on an enhanced cascode-grounded gyrator–C structure, demonstrates independent control of inductance and quality factor through dual tuning mechanisms. The differential version

extends these capabilities by introducing a negative-resistance compensation scheme, which ensures a much higher achievable Q-factor while maintaining a wide inductance tuning range.

Designed in 130 nm CMOS technology, both circuits exhibit favorable characteristics, including high Q values, wideband tunability, low noise, and good linearity. Post-layout simulations and measurements confirm the accuracy of the design methodology and underline robustness under process, voltage, and temperature variations.

The practical advantages of the proposed tunable active inductors will be at the heart of RF and microwave applications where compactness, tunability, and integration are crucial. Their performance makes them attractive candidates for use in reconfigurable filters, LC oscillators, matching networks, and low-noise amplifiers in modern wireless communication systems.

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