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Chapter 4: Novel Tunable Active Inductor Architectures for RF and Microwave Applications

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Abstract: In this chapter, the design, implementation, and performance evaluation of a new TAI architecture in both the grounded and floating configurations are presented. The active-inductor circuit comes in a modified gyrator–C model enhanced by including a passive feedback resistor and a tunable capacitive network. This allows independent tuning of the value of inductance and the quality factor. The floating topology extends these concepts by using cross-coupled transistors that provide negative resistance compensation to further enhance the Q-factor and extend the tuning capabilities of the inductor. The proposed designs are implemented and tested in two different standard CMOS processes (90 nm and 130 nm), where the Cadence® SpectreRF is used for simulation. A wide inductance tuning range, high quality factors (of up to 886 and 388 for the single-ended and balanced active inductors, respectively), excellent noise behavior, and intrinsic robustness against process variations can be achieved. In this context, these structures may be quite beneficial to be integrated in RF and microwave systems, as building blocks for tunable filters, oscillators, and low-noise amplifiers.

Keywords: Active Inductor, Gyrator-C, Grounded AI, Floating AI, Q-Factor, Inductance Tunability, Radio Frequency, Feedback Resistance.

1 Introduction

The demand for compact, reconfigurable, and low-power RF front-ends has further emphasized the role of on-chip inductors. While passive inductors have large area consumption and limited tunability, AIs have emerged as a promising alternative and are characterized by wide tuning capability, compact layouts, and compatibility with modern CMOS processes. However, conventional AI designs are usually limited by low quality factor, poor noise performance, and sensitivity to process variations (Rani et al., 2024).

This chapter presents a novel architecture for tunable active inductors in both the grounded and floating versions. The grounded topology is based on a negative transconductor realized by a common-source stage, a cascaded positive transconductor, and a passive feedback resistor that provides a reduction in series loss as well as an improved Q-factor. An additional auxiliary tunable capacitance has been added to offer flexible inductance tuning while maintaining simplicity in the design.

The floating version extends the grounded design into a differential configuration by interconnecting two grounded AIs with a cross-coupled pair. This configuration generates a controlled negative resistance that compensates parasitic losses, thereby enhancing the quality factor and extending the tuning range. The proposed designs are implemented in commercial CMOS technologies (TSMC® 90 nm and STMicroelectronics® 130 nm) and comprehensively validated through simulation. In fact, performance metrics relevant to practical applications (inductance tunability, quality factor, linearity, noise, process robustness, and power efficiency) are analyzed, proving the state-of-the-art performance of the proposed inductors at low silicon area occupation.

The rest of this chapter is organized as follows: Section 2 describes the design of the grounded active inductor. Section 3 presents its implementation and simulation results. In Section 4, the floating active inductor is introduced with its performance evaluation and sensitivity analysis. Finally, a comparative discussion of the two topologies and their applications to RF and microwave circuits is provided.

2 Design of a Novel Tunable Active Inductor: The Grounded Version

A simplified schematic of the proposed single-ended active inductor is shown in Fig. 4.1 (Saad et al., 2016). The circuit topology is largely based on the standard gyrator–C model and is built around two major blocks: a negative transconductor, implemented by transistor M1 in a common-source configuration, and a positive transconductor, which is realized using transistors M2 and M3 connected as a cascaded differential pair in a common-gate configuration.

To improve performance, an additional passive feedback resistor (R_f) is added between the gate of M1 and the drain of M3. The resistor is made using an n-Poly layer to achieve high resistivity and helps introduce extra impedance that reduces the effective series resistance of the grounded active inductor. A network of tunable capacitors is also added to provide a way to adjust the inductance value independently. Finally, biasing currents I1, I2, and I3 are implemented with NMOS transistors, where the bias voltage V_{bias} controls the current magnitude, allowing greater flexibility in tuning the circuit's behavior.

The circuit is designed with sufficient degrees of freedom to ensure accurate tuning of both the inductance value and the quality factor (Yuan, 2008). Generally, such tuning can be achieved through three mechanisms: resistance adjustment, bias current control using current mirrors, and capacitance variation. In this design, however, the tuning approach relies solely on the capacitive network. This not only simplifies the analytical modeling but also provides a flexible and efficient means of controlling the inductance without adding unnecessary design complexity.

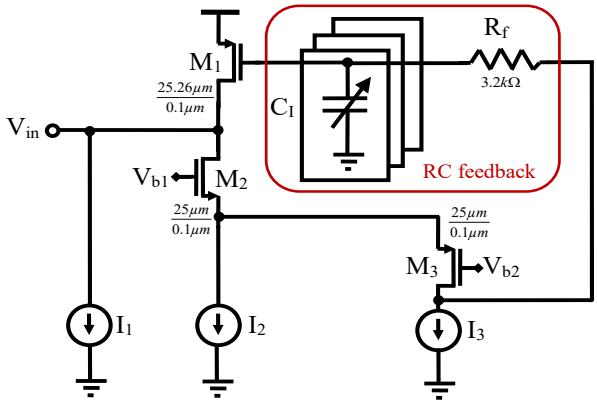


Fig. 4.1 Simplified schematic of the proposed grounded active inductor.

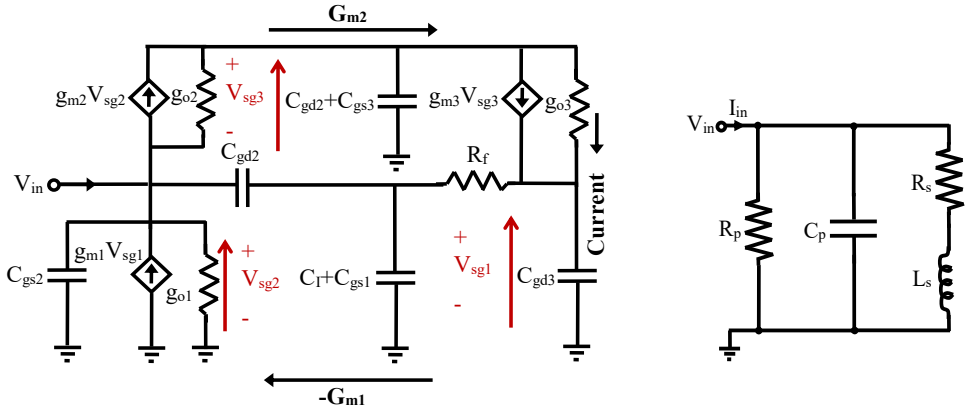
To analyze the behavior of the proposed single-ended active inductor, a small-signal analysis is performed. The extended high-frequency equivalent circuit is depicted in Fig. 4.2, where each transistor is modeled by its main parameters: the gate–source capacitance (C_{gs}), gate–drain capacitance (C_{gd}), transconductance (g_m), and output conductance (g_o). For simplification, transistors M2 and M3 are assumed to be perfectly matched, with identical transconductance, capacitances, and output conductance. Additionally, C_{gd} is considered negligible compared to C_{gs}, and gm is assumed to be much larger than g_o. Under these assumptions, the input admittance of the circuit can be derived, revealing the possibility of resonance.

$$Y_{in}\ ;\ \ sC_{gs}-\frac{C_{gs}}{C_{gs1}+C_I}g_{m1}+g_m+g_{o1}+\frac{1}{s\dfrac{2\left(C_{gs1}+C_I\right)}{g_m g_{m1}}+\dfrac{\dfrac{g_o}{C_{gs1}+C_I}-\omega^2 C_{gs}\left(R_f+\dfrac{1}{g_o}\right)}{g_m g_{m1}}} \quad (91)$$

The resulting expression can be readily mapped to an equivalent parallel RLC network, as illustrated in Fig. 4.2. The parameters of this RLC network are given by:

$$L_s \approx 2\frac{C_{gs1}+C_I}{g_m g_{m1}},\ R_s \approx \frac{\dfrac{g_o}{C_{gs1}+C_I}-\omega^2 C_{gs}\left(R_f+\dfrac{1}{g_o}\right)}{g_m g_{m1}} \quad \text{and} \quad C_p=C_{gs} \quad (92)$$

An important result from this derivation is that the equivalent inductance is independent of the feedback resistance R_f. Instead, R_f primarily reduces series losses and can even lead to negative values of the equivalent resistance R_s, thereby improving the quality factor. The inductance value can also be increased by raising the gate–source capacitance of transistor M1. To achieve this, an auxiliary capacitor (C_I) is added between the gate of M1 and the feedback resistor. In practice, this capacitor is implemented using NMOS varactors controlled by a tuning voltage (V_{ctr}), allowing independent adjustment of the inductance. Alternatively, switched-capacitor arrays, such as MOM or MIM capacitors, can be used to provide fine tuning granularity while maintaining robustness.



(a) (b)

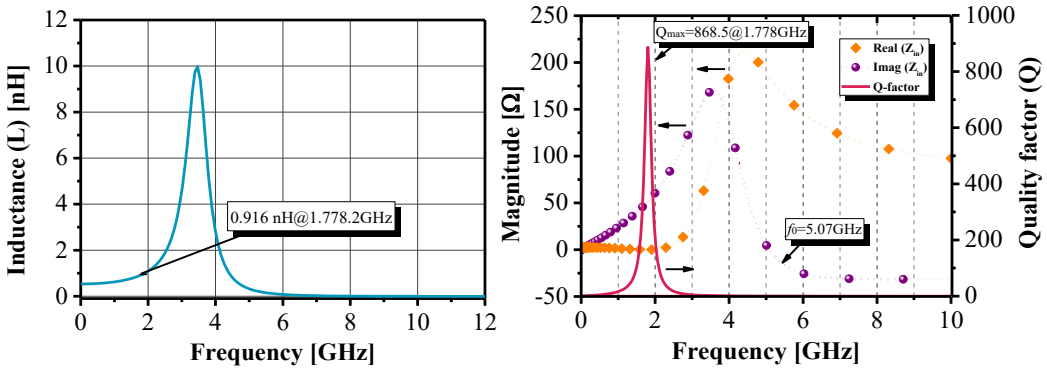
Fig. 4.2 (a) Small-signal equivalent circuit of the proposed grounded active inductor, and (b) its equivalent RLC network.

Some design guidelines can be drawn from the derived relationships. To ensure high-frequency operation with acceptable power consumption, the dimensions of transistors M1–M3 should be kept moderate. The feedback resistor (R_f) plays a key role in optimizing the quality factor: carefully selected values can maximize Q, while excessively large Rf may result in a negative Q, even though the inductive nature is preserved. Additionally, large auxiliary capacitances can significantly degrade the quality factor, emphasizing the need to balance capacitance tuning with performance. The resonant frequency (ω_0) and Q can be calculated as follows:

$$\omega_0 \; ; \; \sqrt{\frac{g_m g_{m1}}{2C_{gs}(C_{gs1}+C_I)}} \qquad \text{and} \qquad Q(\omega_0) \; ; \; \frac{\sqrt{\frac{2g_m g_{m1}(C_{gs1}+C_I)}{C_{gs}}}}{\frac{g_o}{C_{gs1}+C_I} - C_{gs}\omega^2\left(R_f+\frac{1}{g_o}\right)} \qquad (93)$$

In practice, the input admittance can be directly obtained from foundry models using CAD simulation tools, providing a simple and accurate method to confirm the inductive behavior without relying solely on analytical simplifications. As illustrated in Fig. 4.3,

the imaginary part of the input impedance maintains an inductive nature up to about 5 GHz. Simulation results further demonstrate that the proposed design achieves an exceptionally high quality factor, reaching values close to 900.



(a) (b)

Fig. 4.3 Theoretical predictive behavior of the grounded active inductor: (a) equivalent inductance, and (b) Q-factor, real and imaginary parts of the impedance.

3 Design of a Novel Tunable Active Inductor: The Floating Version

The floating version of the proposed active inductor can be implemented using a differential gyrator–C configuration, as shown in Fig. 4.4 (Saad et al., 2022; Saad et al., 2025). Structurally, it consists of two grounded active inductors (TAI-1 and TAI-2) connected by a complementary cross-coupled transistor pair. This cross-coupled stage introduces a controlled negative resistance that compensates for parasitic parallel resistance losses, thereby improving the overall quality factor.

In TAI-1, transistor M1 operates in a common-source configuration to realize the negative transconductance $-g_{m1}$, while transistors M2 and M3 form the positive transconductance g_{m2}/g_{m3}. A current mirror composed of M4–M7 is used to invert the polarity of the transconductance. To further reduce output conductance, the positive transconductor is configured as a cascaded differential common-gate stage, providing better linearity and a wider frequency range of operation. At the differential input, two cross-coupled MOSFET pairs (M9–M′9 and M10–M′10) generate additional negative resistance in parallel with the inductor. This compensation reduces the impact of parasitic resistance on the Q-factor and substantially enhances performance across a broad frequency range. Additionally, a passive feedback resistor R_f is placed between the gate of M1 and the drain of M3 to decrease series loss and increase effective inductance. The use of high-resistivity PMOS devices in this feedback path further strengthens the inductive response without extra power consumption, since the current is effectively reused.

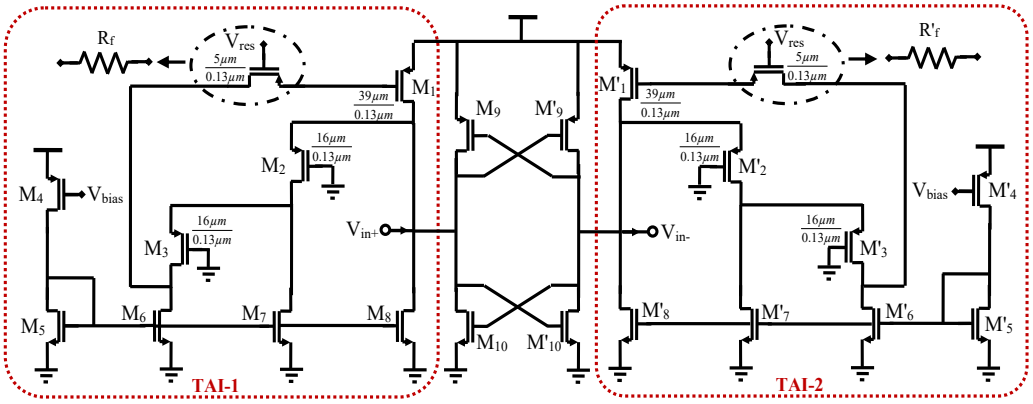


Fig. 4.4 Schematic of the proposed floating active inductor.

The equivalent small-signal model of the differential active inductor is illustrated in Fig. 4.5. Based on this model, the input admittance can be represented by an equivalent RLC network:

$$Y_{in} = -\frac{g_{m9} - g_{m10}}{2} + \frac{R_{tot}}{2} + \frac{sC_{tot}}{2} + \frac{g_m}{2\left(1+sR_{tot}C_{gs1}\right)} \tag{94}$$

where $C_{tot} = C_{gs1} + C'_{gs9} + C'_{gs10}$ and $R_{tot} = r_{ds2} + r_{ds3} + R_f$.

The equivalent RLC parameters are obtained as follows:

$$L_s = \frac{2R_{tot}C_{gs1}}{g_{m1}},\ R_s = \frac{2}{g_{m1}},\ C_p = \frac{C_{tot}}{2} \text{ and } G_p = \frac{-\left(g_{m9}+g_{m10}\right)}{2} + \frac{R_{tot}}{2} \tag{95}$$

The analysis indicates that the feedback resistor R_f enhances the inductance L_s while reducing the parallel resistance R_p.

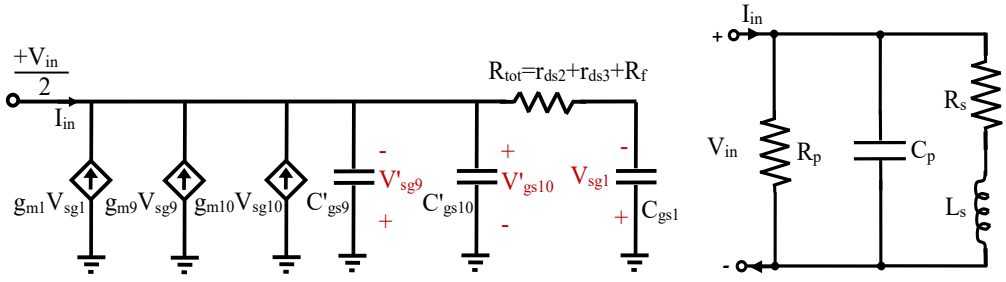


Fig. 4.5 Small-signal equivalent circuit of the floating active inductor.

A critical condition for achieving maximum quality factor occurs when the total resistance from feedback and device parasitics balances the negative resistance produced by the cross-coupled transistors. Under this balance, the circuit reaches a high Q-factor up to frequencies near the self-resonance frequency (SRF). For the floating AI, SRF, zero frequency, and Q-factor are defined as:

$$\omega_0 \approx \frac{1}{\sqrt{L_s C_p}} = \frac{1}{\sqrt{\frac{R_{tot}}{g_{m1}}\left(C_{gs1}^2 + C'_{gs9} + C'_{gs10}\right)}} \tag{96}$$

$$\omega_z = \frac{R_s}{L_s} = \frac{g_{tot}}{C_{gs1}} \tag{97}$$

$$Q\,;\ \frac{R_p}{\omega L_s} = \left| \frac{g_{m1}}{\omega R_{tot} C_{gs1}\left(R_{tot} - g'_{m9} - g'_{m10}\right)} \right| \tag{98}$$

Design insights further show that transistor sizing in the positive transconductance path (M2, M′2, M3, and M′3), as well as the choice of feedback resistors (R_f and R'_f), must be carefully optimized. Oversized devices or excessively large resistors can degrade SRF and increase power consumption. In contrast, moderate device sizing combined with feedback-assisted compensation enables the realization of a floating active inductor with high inductance, low loss, and excellent quality factor, making it well suited for high-frequency analog and RF applications.

3 Implementation Details and Simulation Results of the Grounded Active Inductor

The grounded active inductor was designed and verified using the TSMC 90-nm 1P9M MS/RF CMOS design kit. Circuit-level simulations were conducted with the SpectreRF simulator in the Cadence® design environment, ensuring accurate evaluation of the inductive behavior, quality factor, and frequency response of the proposed topology.

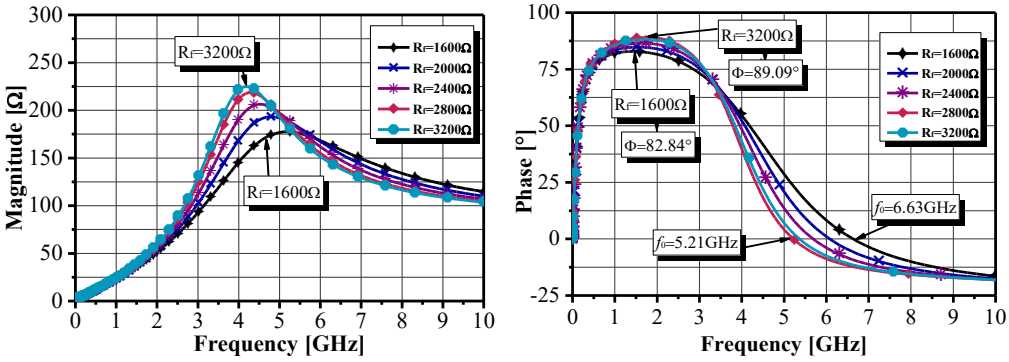
In this section, the performance of the proposed single-ended tunable active inductor (TAI) is analyzed through simulation. The focus is placed on the key parameters that define an active inductor: resonant frequency, inductance tuning range, and quality factor. To further confirm the inductive behavior of the designed circuit, the phase response is studied as a function of the feedback resistance R_f. It is worth noting that this topology has been successfully implemented in both digitally controlled oscillator (DCO) (Saad et al., 2016) and voltage controlled oscillator (VCO) (Saad et al., 2021; Saad et al., 2022) designs, proving its practical feasibility.

The inductance L and quality factor Q are evaluated using the relationships described in (Li et al., 2010):

$$L = \frac{\Im(Z_{11})}{\omega} \qquad \text{and} \qquad Q = \frac{\Im(Z_{11})}{\Re(Z_{11})} \tag{99}$$

3.1 Simulation Results and Performance Analysis of the Grounded Active Inductor

Fig. 4.6(a) and (b) show the simulated real and imaginary parts of the TAI's input impedance, as well as its magnitude and phase response.



(a) (b)

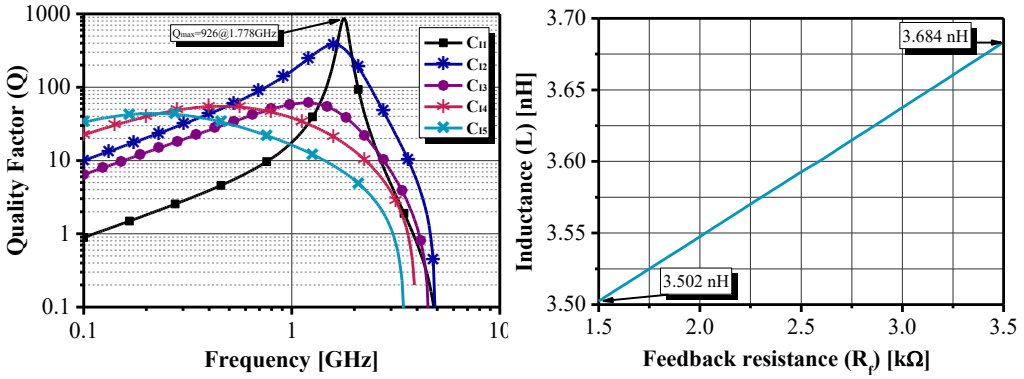
Fig. 4.6 (a) Magnitude, and (b) phase responses of the simulated grounded active inductor.

The circuit demonstrates a clear inductive characteristic across a broad frequency range, extending from about 200 MHz to 6.63 GHz. With a feedback resistor of R_f = 3.2 kΩ, the input impedance phase reaches approximately 90° (89.1°), confirming the expected inductive behavior throughout the operating band. Beyond 6.63 GHz, the imaginary part of the impedance becomes negative, indicating a transition to capacitive behavior.

By optimizing the bias current, the circuit achieves a maximum quality factor of 886.5 at 1.82 GHz, which closely aligns with the theoretically predicted value of 868.5 (see Fig. 4.3(b) and Fig. 4.7(a)). At this frequency, the effective inductance is around 5.2 nH. It is important to emphasize that these results were obtained without activating the auxiliary capacitor C_I, to directly validate the theoretical predictions. Additionally, the relationship between inductance and feedback resistance R_f was examined, showing only a weak dependency with a slope of about 0.1 pH/Ω in the 1.5–3.5 kΩ range (see Fig. 4.7(a)). The design uses a set of NMOS varactors for inductance tuning. The dimensions of the varactors are summarized in Table 4.1.

Table 4.1 Varactor sizes and their corresponding capacitance values as a function of control voltage.

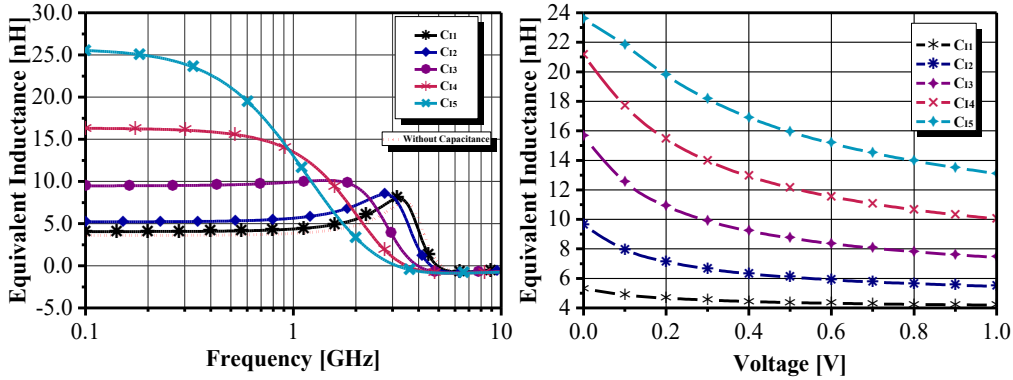
Varactor	Size W/L	Capacitance value (0V to 1V)
C_{I1}	1.0 µm/1.0 µm	09.5 fF-14.24 fF
C_{I2}	2.0 µm/2.0 µm	38.06 fF–58.55 fF
C_{I3}	4.0 µm/4.0 µm	151.59 fF–239.15 fF
C_{I4}	6.0 µm/6.0 µm	340.00 fF–542.39 fF
C_{I5}	8.0 µm/8.0 µm	603.20 fF–968.28 fF



(a) (b)

Fig. 4.7 (a) Quality factor (Q) as a function of frequency and varactor capacitance (C_I), and (b) sensitivity analysis of L to R_f, for the simulated grounded active inductor.

Fig. 4.8 depicts the tuning behavior, indicating that the value of inductance increases considerably with the auxiliary capacitance C_I and lower as a function of the control voltage. Corresponding to the lowest achievable resonant frequency, the inductance reaches 25.53 nH for the maximum designed load capacitance of about 1 pF. However, the circuit linearity tends to degrade during the tuning process. This indeed forms a limitation that can be evident at low operating frequencies when the feedback resistance cannot provide complete compensation for the loss due to the conductance of transistor M1.



(a) (b)

Fig. 4.8 Simulated equivalent inductance value of the grounded active inductor as a function of: (a) different varactor capacitances, and (b) voltage control.

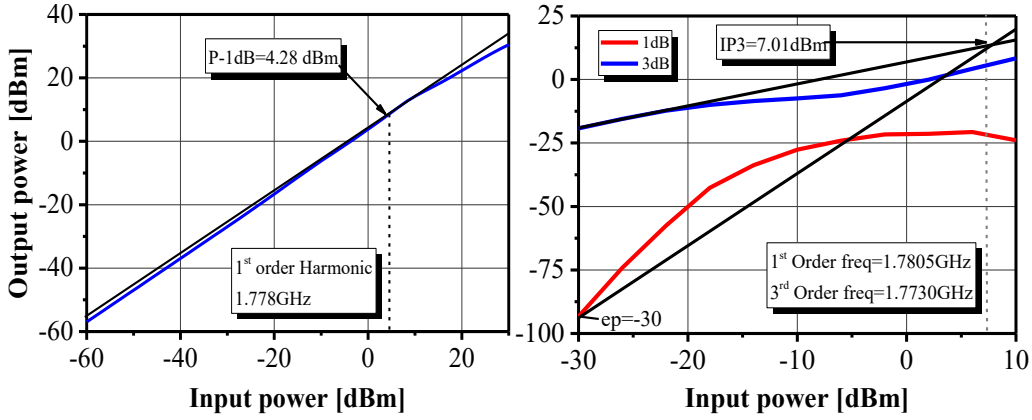
In the following, Table 4.2 summarizes the optimized quality factor together with the SRFs for some selected values of inductances.

Table 4.2 Equivalent inductance (L), quality factor (Q), and self-resonant frequency (SRF) for different varactor values.

Varactor	Q_{max}@f	L@Q_{max}	SRF
C_{I1}	886.5@1778 GHz	5.158 nH	4.87 GHz
C_{I2}	381.8@1.585 GHz	6.385 nH	4.52 GHz
C_{I3}	60.92@1.175 GHz	10.023 nH	3.90 GHz
C_{I4}	56.09@0.467 GHz	15.725 nH	3.37 GHz
C_{I5}	42.85@0.213 GHz	24.785 nH	3.00 GHz

3.2 Linearity and Noise Analysis

Another important feature of the design being proposed here is that of linearity, although this is rarely explicitly addressed in active inductor studies that have appeared in the literature. Linearity has been assessed using the approach described in Ref. (Abdalla et al., 2007). Here, an input port excitation with an RF signal may be used to excite the circuit under consideration and thus give rise to harmonic responses. In the case of the TAI proposed here, an input 1-dB compression point of 4.28 dBm has been obtained. Correspondingly, this represents an input voltage swing of approximately 1.03 V for a 1.0-V supply. Additionally, the circuit exhibits a third-order input intercept point (IIP3) of 7 dBm. Shown in Fig. 4.9, these results confirm that the grounded TAI combines high inductance tunability and quality factor with competitive linearity performance.



(a) (b)

Fig. 4.9 Linearity performance of the grounded AI: (a) 1-dB compression point (P−1dB), and (b) third-order intermodulation intercept point (IIP_3).

Fig. 4.10 shows the output noise variation with frequency. The grounded AI has an equivalent output noise voltage of 13 nV/√Hz. This is significantly lower than the 21 nV/√Hz obtained in the conventional active inductor model without feedback and

compares well with the 12 nV/√Hz obtained when a feedback transistor is used, as shown in Ref. (Manjula et al., 2013). The above results clearly demonstrate that the proposed design indeed presents a good noise performance, in addition to the favorable characteristics of its tunable architecture.

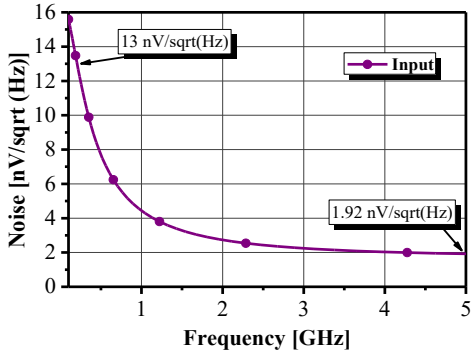
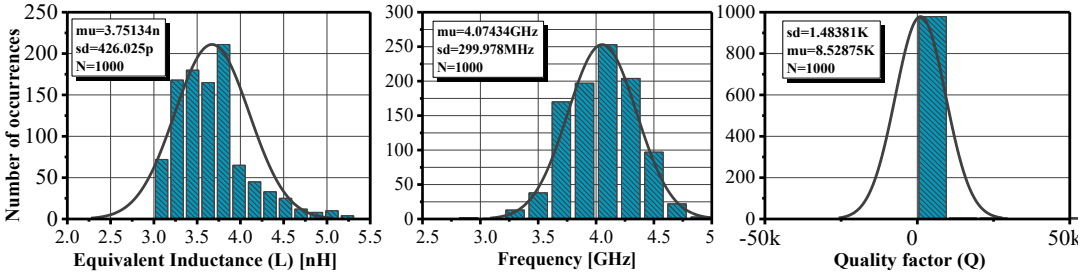


Fig. 4.10 Noise performance of the grounded AI.

3.3 Sensitivity to Process Variations and Stability Assessment

To verify the robustness of the proposed grounded AI against process variation and device mismatch, 1000-iteration Monte Carlo simulations are carried out. The statistical distributions of inductance, quality factor, and SRF are shown in Fig.4.11. The results are summarized in Table 4.3. It is worth noting that the quality factor is greatly affected by process variation unless the feedback resistance R_f is kept constant. For a given C_I, from the Gaussian distribution at the ±3σ confidence level, 98.5% of the inductance values are in the range of 3–5 nH. Similarly, 97.5% of the SRF values fall between 3.18 and 4.68 GHz. It can be concluded that both L and ω0 have relatively good process tolerance, with 13.5% and 6.66% of 3σ variation compared to their mean values, respectively. Such a robustness is particularly desirable in both filter and oscillator designs, wherein an accurate resonant frequency is often a crucial design specification.



(a) (b) (c)

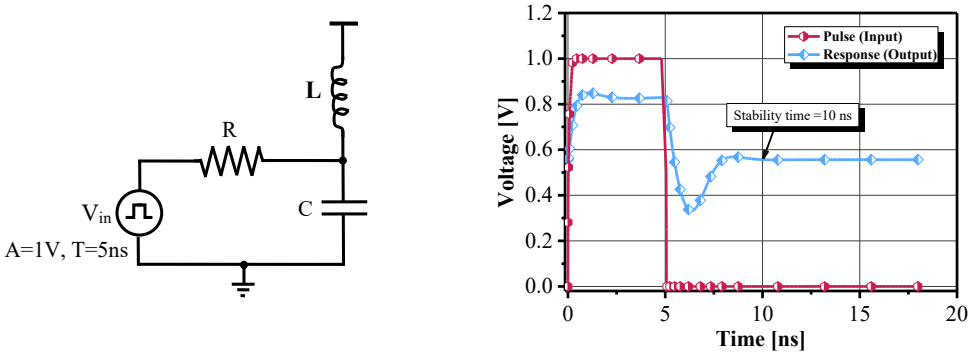
Fig. 4.11 Monte Carlo analysis of the grounded AI: (a) equivalent inductance, (b) self-resonant frequency (SRF), and (c) quality factor (Q).

Table 4.3 Performance of the grounded AI due to process and mismatch effects

Type	Equivalent inductance [nH]	Q-factor	SRF [GHz]
Mean (μ)	3.813	378.5	4.036
Standard deviation (σ)	0.515	740.4	0.296
σ/μ	13.5%	195%	6.66%
Minimum	3.341	4.7	3.388
Maximum	5.189	2542	4.365

N = number of iterations (1000).

Finally, stability considerations were addressed during the design process. Since the TAI architecture incorporates a feedback resistance in combination with an inverting operational transconductance amplifier (OTA), it exhibits a loop structure. As a result, a standard linear stability analysis cannot be applied to this one-port network as the stability analysis technique based, for example on the Rollet stability factor, is inapplicable (Manjula et al., 2013). Alternative approaches must therefore be employed in order to ensure reliable operation. To further demonstrate its applicability, the grounded AI was embedded in an RLC resonant circuit as shown in Fig. 4.12(a) (Cho et al., 1997). The transient analysis of this configuration was carried out using a high load resistance of R=1 MΩ and an input pulse of 5 ns. The simulated response shows that the circuit stabilizes within 10 ns (See Fig. 4.12(b)).



(a) (b)

Fig. 4.12 (a) Stability test circuit, and (b) Its corresponding response.

3.4 Layout and Power Consumption

The grounded AI is biased from a single 1V supply. Due to the limited number of transistors in the design, its peak power consumption for the active inductor core is only 0.515 mW, which is highly suitable for low-power RF applications. The physical layout of the circuit in Fig. 4.13 takes only 605 μm² area, which again justifies the efficiency of the implementation both regarding power and silicon area.

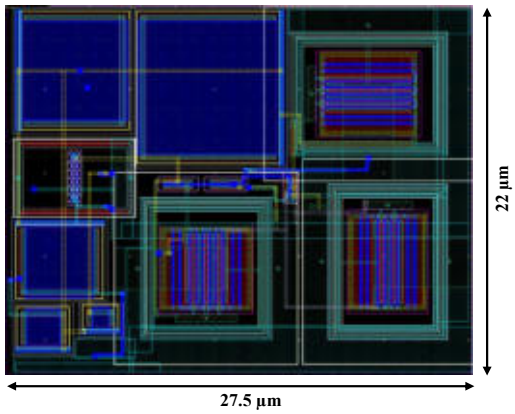


Fig. 4.13 Layout of the grounded active inductor (AI).

4 Implementation Details and Simulation Results of the Floating Active Inductor

This paper presents the floating active inductor, which is implemented by using the 130 nm CMOS technology of STMicroelectronics©. Circuit simulations are carried out in the Cadence® design environment with the Spectre-RF© simulator. This choice gives a good balance between the performance of the devices and the flexibility in the design, allowing reliable evaluation of the differential inductor topology.

4.1 Simulation Results and Performance Analysis of the Floating Active Inductor

The main performance metrics of the DAI are considered in terms of effective inductance tuning, L, quality factor Q, and resonance frequency f_0. Also, to validate further the inductive behavior of the topology, the phase response under different values of feedback resistance R_f is analyzed (Saad et al., 2025).

Characterization of this version of the AI is done using a two-port S-parameter analysis. Following the procedure in Ref. (Ler et al., 2008), L and Q are calculated using Equations (100–101):

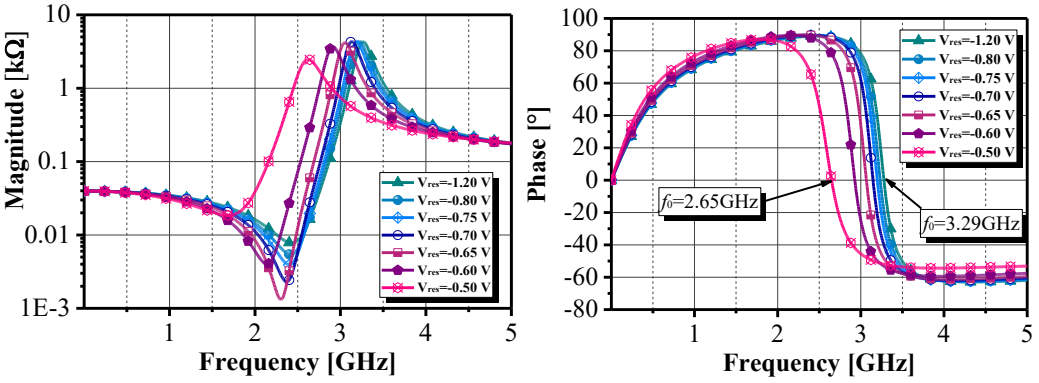
$$Z_{diff} = Z_{11} - Z_{21} - Z_{12} + Z_{22} \tag{100}$$

$$L = \frac{\Im m(Z_{diff})}{\omega} \quad \text{and} \quad Q = \frac{\Im m(Z_{diff})}{\Re e(Z_{diff})} \tag{101}$$

The variation of the active resistance R_f is obtained for the control voltage V_{res} ranging from –0.3 V to –1.2 V. The frequency response of the input impedance Z_{in}, magnitude and phase, is depicted in Fig 4.14 for various values of V_{res}. The real and imaginary parts of Zin evolution are shown in Fig. 4.15. It is found that an increase in V_{res} is accompanied

by a decrease in both resonant frequency f_0 and zero frequency f_z. The circuit exhibits an inductive behavior in frequency range starting from few megahertz up to around 3.3 GHz. For V_{res} equal to –0.7 V, the impedance phase has a value close to 90° (~89.85°) throughout the operation band, which confirms the inductive nature of the structure. Beyond 3.3 GHz, the imaginary part of Z_{in} becomes negative, and hence the circuit shows a capacitive behavior, as also mirrored by the phase response (see Fig. 4.14).

The Q-factor and resonance frequency are plotted as a function of V_{res} in Fig. 4.16(a). Tuning of the quality factor is further emphasized in Fig. 4.16(b) between control voltages –0.5 V and –0.8 V. As expected, the resonant frequency ω_0 is inversely proportional to $\sqrt{V_{res}}$. A maximum quality factor of 388 is obtained at 2.31 GHz. This is well above the required values for typical RF applications. The variation of the equivalent inductance with R_f is also assessed. From Fig. 4.16(b) it follows that the inductance varies between 33 nH and 98 nH for a sweep of V_{res} from –0.3 V to –1.2 V.



(a) (b)

Fig. 4.14 Magnitude and phase response of the floating active inductor as a function of the control voltage V_{res}.

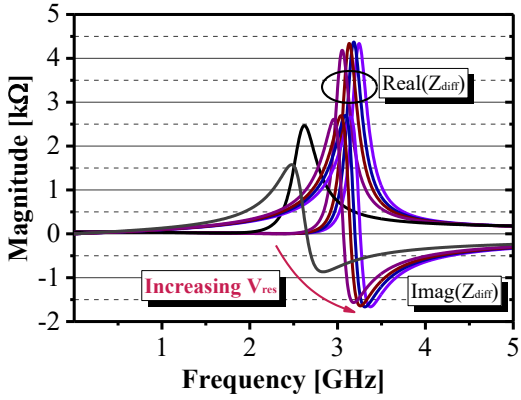


Fig. 4.15 Real and imaginary components of the input impedance of the floating AI, showing inductance tuning across various V_{res} levels.

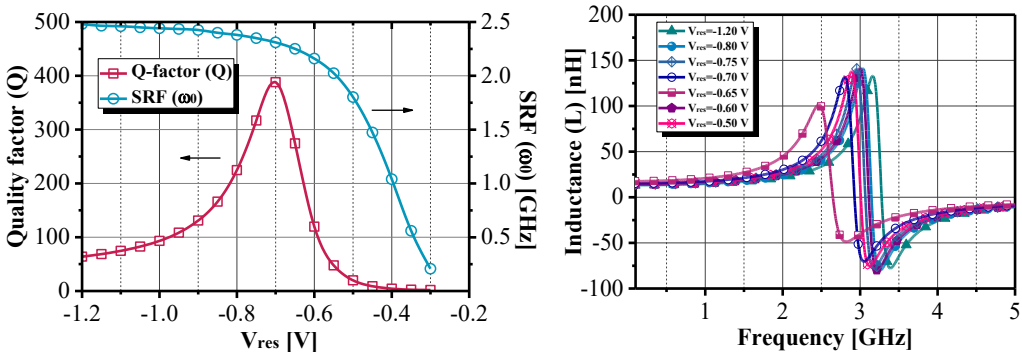


Fig. 1.16 (a) $\omega_0$and Q tuning as a function of V_{res}, and (b) equivalent inductance vs. frequency for various V_{res} levels.

4.2 Noise and Linearity Performance of the Floating AI

Fig. 4.17 shows the input-referred noise characteristics of the floating AI. Here, it can be noted that the input-referred noise level decreases with increasing SRF. The obtained noise for SRF greater than 1 GHz remains below 3.3 nV/√Hz, showing a good agreement with the noise levels reported for other state-of-the-art active inductors (Grozing et al., 2001; Vema Krishnamurthy et al., 2010; Kumar et al., 2017; Chu et al., 2025).

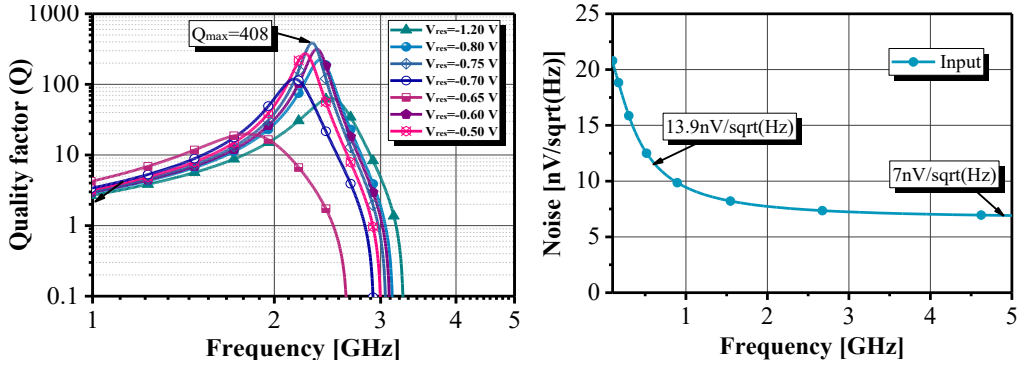


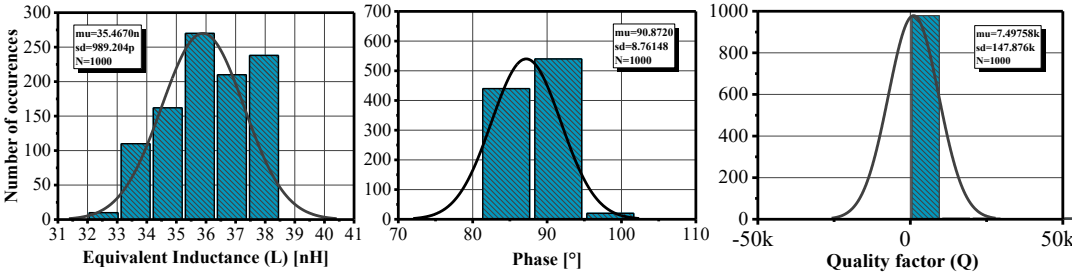
Fig. 4.17 (a) Quality factor (Q) as a function of frequency and control voltage (V_{res}), and (b) noise response.

Moreover, the linearity of the floating differential active inductor has been characterized based on the approach in Refs. (Ler et al., 2009; Li et al., 2010). Two RF signal sources were injected onto the differential input ports to produce harmonic components. The circuit exhibits an input 1-dB compression point (L-1dB) of 2.25 dBm, reflecting a differential input voltage swing of about 0.82 V for a 1.2 V supply voltage. Additionally, a third-order input intercept point (IIP3) of 9.71 dBm is achieved, validating the linearity capability of the proposed design.

4.3 Sensitivity to Process Variations: Monte Carlo Analysis

Monte Carlo simulations were performed on the floating AI to assess its robustness due to both process variations and device mismatch; 1000 runs were run. Results of effective inductance, quality factor, self-resonant frequency, and phase are summarized in Fig 4.18 and Table 4.4.

It is found that the phase response and Q-factor are highly sensitive to process and mismatch variations, unless the tuning voltage V_{res} is set to a fixed value. Curiously enough, this large variation of Q can be used partly to compensate for the process deviations. In contrast, both the effective inductance and the SRF show a very robust behavior against variation, with standard deviations amounting to only 2.79% and 7.08%, respectively, of their mean values.



(a) (b) (c)

Fig. 4.11 Monte Carlo analysis of the floating AI: (a) equivalent inductance, (b) self-resonant frequency (SRF), and (c) quality factor (Q).

Table 1.4 Performance of the floating AI due to process and mismatch effects

Type	L [nH]	Q-factor	SRF [GHz]	Phase [°]
Mean	35.467	7497	2.332	90.87
Standard deviation (σ)	0.989	147 876	0.165	8.76
σ/mean	2.79%	5.07%	7.08%	9.64%
Minimum	32.48	5.275	2	79.37
Maximum	38.63	4.6 106	3.07	177.5

Total number of iterations/hits = 1000, evaluated at V_{res}=-0.7V

This robustness is further verified by the statistical distribution: within a confidence interval of ±3σ, about 98.5% of the SRF samples fall within the frequency range of 2.002–2.827 GHz, and 98.5% of the inductance samples lie between 32.5 and 38.4 nH. Such stability in L and ω_0 will be very beneficial when integrating the inductor into oscillator and LNA designs that need accurate frequency control.

4.4 Layout and Power Consumption

This differential version active inductor is designed to operate from a single 1.2V supply, making it compatible with low-voltage CMOS processes. Thanks to using a moderate transistor count, the core circuit consumes a maximum of 7.28 mW of power, confirming its suitability for energy-constrained RF applications. The layout implemented in Fig. 4.19 occupies only 855 µm² of silicon area. This realizes an efficient design both in terms of power efficiency and area.

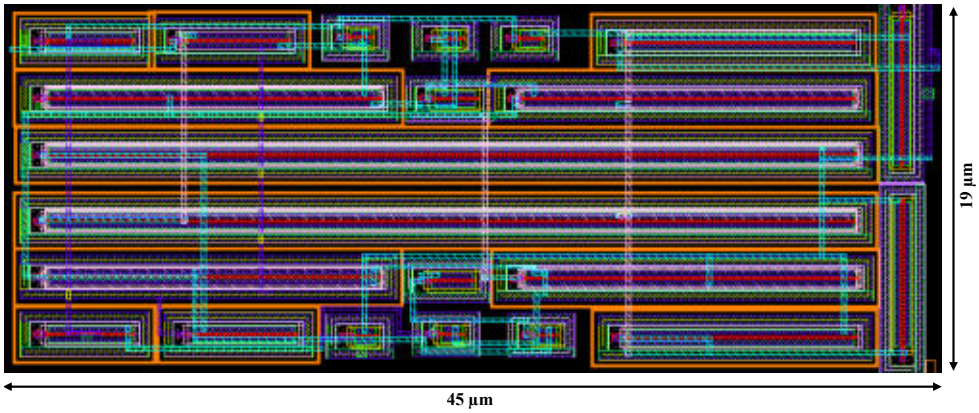


Fig. 4.19 Layout of the floating active inductor (AI).

Conclusion

This chapter has discussed and presented two new tunable active inductor architectures in both grounded and floating configurations that have been designed and simulated in standard CMOS technologies. The grounded version exhibits exceptional tunability and a very high quality factor of almost 900, while area and power consumption remain very small. It is highly suitable for adaptive RF circuits due to its tunable capacitive network that allows easy control of inductance value.

The floating version, with a differential gyrator-C structure with cross-coupled negative resistance compensation, achieves wide inductance tuning, robust Q-factor enhancement, and competitive noise and linearity performance. It offers higher robustness to parasitic effects and an improved differential-mode operation, although at the price of somewhat increased power consumption with respect to the grounded topology, making it of particular interest for oscillators, LNAs, and impedance-matching networks.

Both implementations are tolerant of process variations, and inductance and resonant frequency have been proven to be stable against fabrication tolerances through Monte Carlo analysis. The grounded implementation is preferred for ultra-low-power

applications with highly restricted area constraints, while the floating implementation has better performance in wideband high-linearity RF systems.

In brief, the proposed tunable active inductors represent an advance in the state of the art by integrating high Q, wide tuning range, noise efficiency, and process robustness within compact CMOS realizations. Their features make them strong candidates for next-generation RF and microwave applications, notably in reconfigurable filters, voltage-controlled oscillators, and multi-standard transceivers.

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