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Chapter 3: Recent Advances in Single-Ended Gyrator–C Active Inductor Designs (Innovations from 2008)

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Abstract: This chapter reviews the developments of single-ended gyrator-C active inductors from 2008 to the present. Based on the foundational work summarized in Ref. (Yuan, 2008), the discussion focuses on state-of-the-art CMOS implementations aimed at overcoming persistent challenges such as low quality factor, nonlinearity, high power consumption, and limited tunability. Each subsection highlights significant advancements, including improvements in transconductance and feedback architectures, as well as innovations in biasing, noise reduction, and layout optimization. Together, these developments demonstrate the ongoing evolution of active inductors toward becoming practical, high-performance alternatives to passive on-chip inductors, particularly for RF filters, oscillators, and impedance-matching networks in nanoscale CMOS technologies.

Keywords: Active Inductor, Gyrator-C, Single-Ended, Optimization, CMOS, Radio Frequency (RF), Integrated Circuit.

1 Introduction

This chapter overviews recent topologies and implementations of CMOS active inductors, focusing on single-ended gyrator–C configurations introduced since 2008. The discussion centers on circuit architectures and the performance enhancement techniques developed over the past decade, outlining their design concepts, advantages, and trade-offs.

Earlier works, especially active inductor circuits published before 2008, were comprehensively analyzed by Professor Fei Yuan in his seminal book *CMOS Active Inductors and Transformers: Principle, Implementation, and Applications* (Yuan, 2008). Building on that foundation, this chapter continues the discussion by emphasizing

developments that either refine or diverge from classical methods to meet the requirements of modern RF and mixed-signal systems.

Since 2008, the scaling of CMOS technologies and the rise of multiband, multifunctional communication systems have driven the need for compact, reconfigurable inductive components. Single-ended gyrator–C active inductors remain a key research topic due to their simplicity, wide tunability, and adaptability to diverse circuit contexts. However, their performance has long been limited by low Q-factors, high noise, and poor linearity. To overcome these issues, researchers have proposed several solutions, including feedback-resistance tuning, cascode-based designs, auxiliary capacitive loading, current-reuse topologies, adaptive biasing, and hybrid passive–active approaches.

The chapter organizes these advances both chronologically and thematically to provide a clear overview of key milestones and innovations. Sections 2.1 through 2.17 examine notable active inductor architectures proposed by researchers such as Ghadiri-Moez, Bhattacharya, Rafei-Mosavai, Lai-Zheng, and Tang, each representing a significant step toward the practical and efficient use of active inductors in nanoscale CMOS. Particular emphasis is placed on how these designs enhance inductance, Q-factor, noise, and linearity while meeting the constraints of low-voltage, low-power operation.

2 Recent Advances in Single-Ended Gyrator–C Active Inductor Designs: Design Innovations and Optimization Techniques (2008–Present)

Over the last fifteen years or so, single-ended gyrator–C active inductor (AI) topologies have undergone significant evolution, driven by increasing demands for compact, tunable, and high-performance on-chip inductive components in RF and mixed-signal circuits. This section reviews major post-2008 innovations, examining their conceptual foundations, implementation approaches, and their influence on key performance parameters such as inductance tuning range, Q-factor improvement, stability, and suitability for integration within modern CMOS technologies.

2.1 Ghadiri-Moez Active Inductor

Ghadiri and Moez proposed a CMOS active inductor topology, as shown in Fig. 3.1, which was used for the design of a phase shifter for UWB applications (Ghadiri & Moez, 2014). The structure is based on a conventional cascode active inductor topology, where transistor M3 is stacked over M1. This stacking improves the gain of the cascode amplifier while it reduces the parasitic series resistance of the active inductor for a better quality factor, Q. The wide linear inductive response makes it suitable for broadband circuit applications.

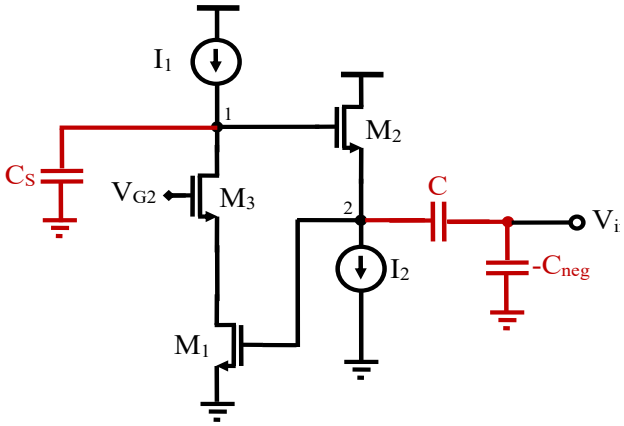


Fig. 3.1 Simplified schematic of Ghadiri-Moez active inductor.

Despite these benefits, the design process is complex. The nonlinear behavior of MOS transistors, stemming from their intrinsic resistive and capacitive parasitics, causes the input impedance and admittance to vary nonlinearly with frequency. To simplify the analytical modeling, the gate–drain capacitance (C_{gd}) and other parasitic capacitances are neglected. Assuming transistors M1, M2, and M3 are identical devices, the input admittance of the active inductor can be expressed as:

$$Y_{in} = sC_{gs} + g_m + \frac{R_{ds}g_m^2}{sR_{ds}\left(C_{gs}+C_s\right)+1} \tag{43}$$

From this expression, the equivalent RLC model parameters can be derived as follows:

$$C_p = C_{gs} \tag{44}$$

$$R_p = \frac{1}{g_m} \tag{45}$$

$$L_s = \frac{C_s + C_{gs}}{g_m^2} \tag{46}$$

$$R_s = \frac{1}{R_{ds}g_m^2} \tag{47}$$

It follows from (47) that the series resistance R_s has no influence on the frequency-dependent behavior of the active inductor. Based on definition of frequency dependency, FD, introduced in (Ghadiri & Moez, 2014), and assuming $\omega R_{ds}C_{gs}>>1$, the FD percentage of the circuit reads:

$$\left|\mathrm{FD}(\%)\right| \approx 100 \times \frac{\omega^2 \mathrm{LC}_{gs}}{1\text{-}\omega^2 \mathrm{LC}_{gs}} \tag{48}$$

Here, $L=-(C_S+C_{gs})/g_m^2$ and C_S represents the negative load capacitance of the active inductor. Eqn. (48) shows that to minimize the %FD, i.e. reducing the deviation from the desired value of inductance, the value of C_S and the gate–source capacitances of the transistors need to be reduced. Thus, the sizing of transistors M1 and M2 should therefore be optimized carefully, therefore trading off %FD and the desired value of inductance.

The circuit was fabricated in IBM's® 0.13-μm, 1.5-V CMOS process. Simulation results reported in (Ghadiri & Moez, 2014) show the maximum operational bandwidth is 10.3 GHz. The fabricated prototype is frequency-independent for a maximum frequency of 7.8 GHz and a maximum Q-factor of 45. The total power consumption of this topology is 21 mW.

2.2 Bhattacharya Active Inductor

There are several advantages of the Thanachayanont-Payne active inductor architecture:

- An independently adjustable upper bound of the frequency range;
- Enhanced quality factor due to improved parasitic parallel resistances and reduced parasitic series resistance;
- An inductance value that is almost constant over a wide frequency band.

While these characteristics are desirable, one of the significant disadvantages of this topology is its inability to maintain linearity under high power input. Bhattacharya et al. have developed an active inductor topology that avoids this weakness, as shown below (Bhattacharya et al., 2015). An implementation of the Bhattacharya active inductor by using two transconductors is shown in Fig. 3.2.

This circuit topology consists of one common-source stage, transistor M1, which is configured to provide negative transconductance, followed by the second common-source transconductor (transistor M2) with positive transconductance. Another transistor, M3, connected in common-source mode, too, is put in shunt between the feedback resistor and M2. This additional device allows applying the feed-forward current source (FFCS) technique, described by Ler et al. (Ler et al., (2009), as an effective means for reducing large-signal gm variation. With properly scaled device dimensions, transistors M2 and M3 can be designed in such a way that dynamic variations in the drain current of M2 are canceled out, which suppresses the nonlinear effects, thus improving linearity for the active inductor.

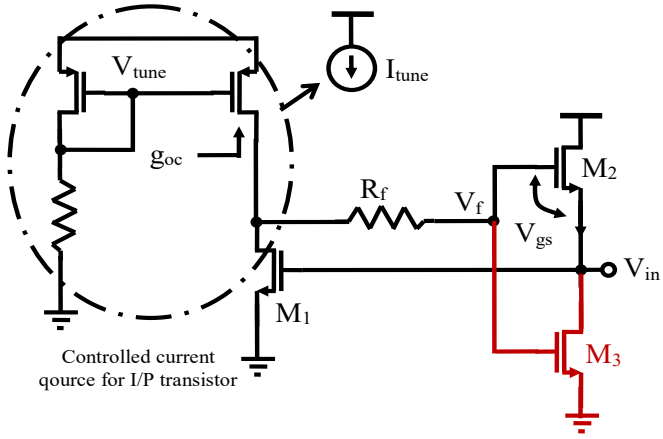


Fig. 3.2 Simplified schematic of Bhattacharya active inductor.

2.3 Rafei-Mosavai Active Inductor

A feedback resistor improves the performance of an active inductor by a considerable margin. Such an element can provide compensation for series losses, giving a good quality factor and increasing effective inductance. Based on this, Rafei and Mosavai proposed a feedback RC active inductor that can further reduce series loss (Rafei & Mosavai, 2013) as shown in Fig. 3.3.

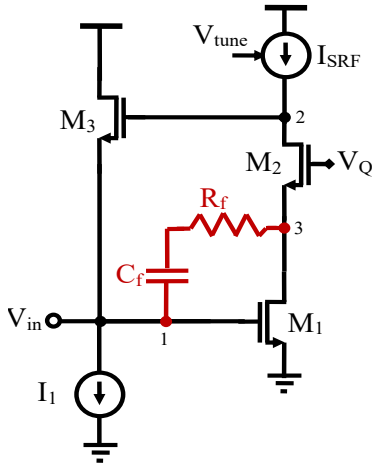


Fig. 3.3 Simplified schematic of Rafei-Mosavai active inductor.

Without the RC feedback, the equivalent RLC parameters for the Rafei–Mosavai active inductor can be calculated by analyzing the circuit impedance under the assumption g_{ds}=0. This gives:

$$Z_{in} = \frac{sC_{gs3}}{s^2 C_{gs1} C_{gs3} + sC_{gs3} g_{m1} + g_{m1} g_{m3}} \tag{49}$$

Equation (49) can be represented in a parallel RL network form as:

$$R_p = \frac{1}{g_{m1}} \tag{50}$$

$$C_p = C_{gs1} \tag{51}$$

$$L_p = \frac{C_{gs3}}{g_{m1} g_{m3}} \tag{52}$$

The self-resonant frequency can be determined as:

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} = \sqrt{\frac{g_{m1} g_{m3}}{C_{gs1} C_{gs3}}} = \sqrt{\omega_{t1} \omega_{t3}} \tag{53}$$

From equation (52), it is obvious that the value of inductance does not change from that of the conventional active inductor. The self-resonant frequency can be improved by scaling g_{m1} and g_{m3}, which, through the transconductance to capacitance relationship, can be used to scale the parasitic capacitances C_{gs1} and C_{gs3} in equation (53). The penalty is a smaller parasitic parallel resistance R_p in equation (53) that sets the bound on the Q-factor of the inductor. Here the effect of the series resistance R_s is usually negligible since R_p is dominant. The Q-factor, therefore, is:

$$Q = \frac{R_p}{\omega L_p} = \frac{\omega_{t3}}{\omega} \tag{54}$$

where denotes the cut-off frequency of transconductor.

where the cut-off frequency of transconductor $\omega_{ti} = g_{mi} / C_{gsi}$, i=1, 2, 3 .

In practical design, R_p should be maximized, while the parallel capacitance C_p is minimized in order to maintain a strong inductive behavior.

If an RC feedback network is introduced in the forward path and precisely between the drain and gate of the transistor M1, then the input admittance of the structure, as proposed by Rafei and Mosavai, is given by:

$$Q = \frac{R_p}{\omega L_p} = \frac{\omega_{t3}}{\omega} \tag{55}$$

$$Y_{in} = \frac{C_{gs3}g_{m1} - C_f g_{m3}}{C_{gs3}} + \frac{g_{m1}g_{m2}}{sC_{gs3}} \tag{56}$$

Equation (56) shows that the RC feedback active inductor can be represented by an inductance in parallel with a resistance as:

$$R_p = \frac{C_{gs3}}{C_{gs3}g_{m1} - C_f g_{m3}} \tag{57}$$

$$L_p = \frac{C_{gs3}}{g_{m1}g_{m2}} \tag{58}$$

From Equation (57), equivalent parallel resistance increases substantially by tuning $C_f g_{m3}$ close to $C_{gs3}g_{m1}$.

The topology can be converted to its equivalent series RL model for further insight. The parameters are defined by:

$$R_s = \frac{C_{gs3}\omega^2\left(C_{gs3}g_{m1} - C_f g_{m3}\right)}{\left(C_{gs3}g_{m1} - C_f g_{m3}\right)^2\omega^2 + \left(g_{m1}g_{m3}\right)^2} \tag{58}$$

$$L_s = \frac{C_{gs3}g_{m1}g_{m3}\omega}{\left(C_{gs3}g_{m1} - C_f g_{m3}\right)^2\omega^2 + \left(g_{m1}g_{m3}\right)^2} \tag{59}$$

Equation (58) indicates that Rs can be made nearly zero while preserving the inductive behavior. The resulting quality factor then is:

$$Q = \frac{\omega L_s}{R_s} = \frac{R_p}{\omega L_p} = \frac{g_{m1}g_{m3}}{\omega\left(C_{gs3}g_{m1} - C_f g_{m3}\right)} \tag{60}$$

It results from (60) that choosing $C_f g_{m3} = C_{gs3}g_{m1}$ yields theoretically an infinite Q-factor.

One of the salient features of the Rafei-Mosavai topology is that the self-resonant frequency ω_0 and quality factor Q can be tuned independently. The resonant frequency can be set through g_{m1} and g_{m3}, by means of the bias ISRF, whereas the Q-factor is varied through g_{m2} via V_Q. In practice, though, variation in $\omega 0$ generally needs to be followed by readjustment of Q. Simulation results for a 90 nm CMOS implementation in (Rafei & Mosavai, 2013) show a Q-factor as high as 13,159 at an inductance of 2.2 nH and 6.6 GHz.

2.4 Lai-Zheng Active Inductor

Techniques of negative resistance are one of the efficient methods to minimize the effect of MOSFET parasitic resistances on the quality factor of an active inductor. The configuration proposed by Lai and Zheng, Fig. 3.4, utilizes this principle for improving inductor performance (Lai & Zheng, 2011). A positive transconductance, g_{m1}, provided by transistors MN1 and MP1, makes up the topology along with a negative transconductance, g_{m2}, which is realized using transistors MN2, MP2, MN3 and MP3.

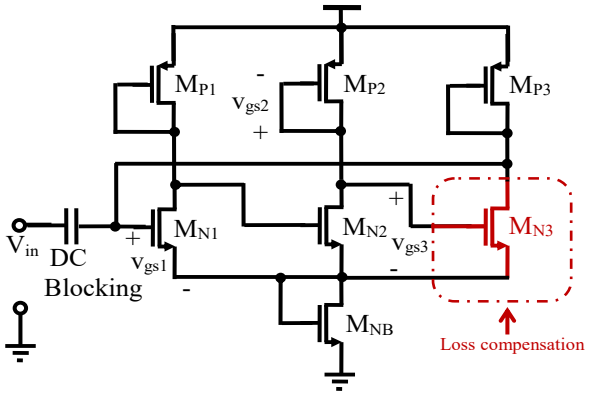


Fig. 3.4 Schematic of Lai-Zheng active inductor.

This can be achieved through a negative resistance circuit by transistor MN3 in association with an auxiliary capacitor that has the function of blocking the DC component of the current. The equivalent negative resistance is given by:

$$R_n = \frac{v_{in}}{v_{gs3} g_{m3}} = \frac{-1}{g_{m3}\left(\frac{-v_{gs3}}{v_{gs1}+v_{gs2}-v_{gs3}}\right)} \tag{61}$$

where v_{gsi} are the gate-to-source voltages of transistors MN1, MP2 and MN3 respectively.

It follows from expression (61) that the value of negative resistance is proportional to v_{gs3}. In order for the circuit to present the positive inductance L and remain in the area of negative feedback stability, the condition $v_{gs1}+v_{gs2}>v_{gs3}$ must be satisfied.

The Lai-Zheng active inductor was successfully applied to microwave notch filter designs and was analyzed by the Agilent Advanced Design System® (ADS) (Lai-Zheng, 2011) to show the possibility of negative resistance compensation in improving the performances of active inductors at high frequencies.

2.5 Tang Active Inductor

The performance of the active inductors can be further improved by stabilizing the input signal swing that leads to a reduction of distortion and enhancement of linearity. For improving the Q-factor of Wu's AI, (Wu et al. 2001), Tang's AI. (Tang et al., 2008; Tang et al., 2009) proposed the addition of a feedback current network as shown in Fig. 3.5.

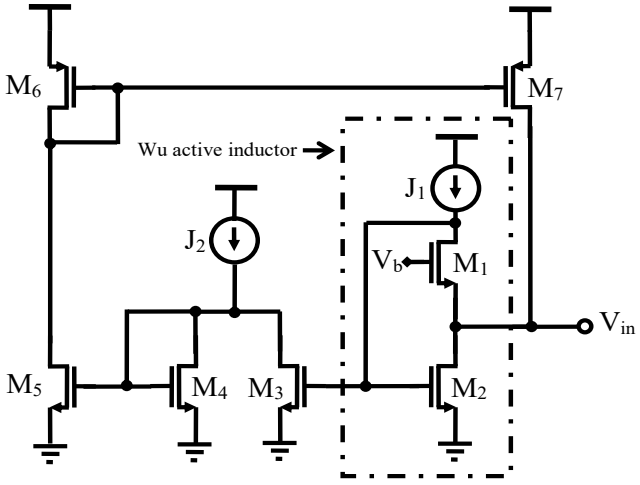


Fig. 3.5 Schematic of Tang active inductor.

In this configuration, the RLC equivalent circuit parameters are similar as in the original design given by $C_p=C_{gs2}$, $R_p=g_{m2}$, $L_s=C_{gs1}/g_{m1}g_{m2}$ and $R_s=g_{o1}/g_{m1}g_{m2}$. The quality factor is given in (Yuan, 2008):

$$Q=\frac{\omega}{R_s}\frac{R_p}{R_p+R_s\left[1+\left(\frac{\omega L}{R_s}\right)^2\right]}\left(1-\frac{R_s^2}{L}-\omega^2 LC_p\right) \tag{62}$$

It is noticeable from (62) that these parameters are functions of C_{gs1}, C_{gs2}, g_{m1}, and g_{m2}, which are determined by the channel currents of transistors M1 and M2. An extra current source, J2, is added so that both the Q-factor and the inductance are kept invariant and large input current swings have minor influence on $J1+I_{in}$.

In practical design, J2 is often set to equal the maximum expected input-current swing I_{in}. Therefore, transistor M7 injects a negative-feedback drain current into the input terminal $I_{D7}=I_{in}-I_{D2}$ for maintaining the drain current I_D of transistor M2 almost constant. Consequently, an improved Q stability of the circuit at high input-signal levels can be achieved.

2.6 Vema Krishnamurthy Active Inductor

Vema Krishnamurthy et al. proposed an active inductor architecture featuring thermal-noise cancellation (NC) through a feedforward stage (Vema Krishnamurthy et al., 2010). In the design, the positive transconductance is implemented with a differential pair of transistors M1 and M2, and the negative transconductance is provided by another differential transistor pair, M3 and M4. In the feedback path, there is also a degeneration resistor R_f to increase the performance. The simplified schematic of the proposed topology is shown in Fig. 3.6.

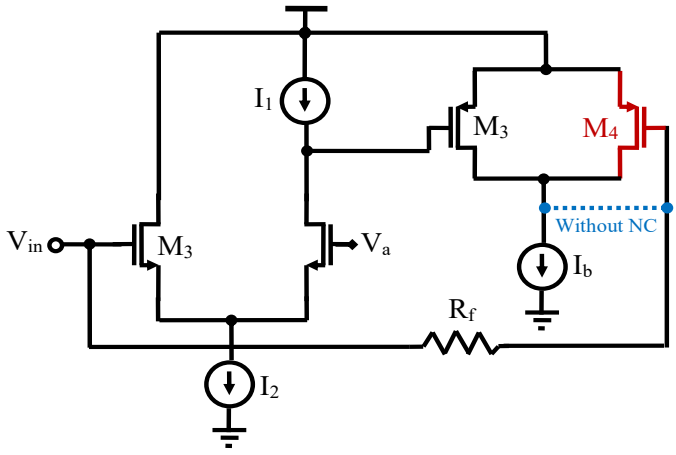


Fig. 3.6 Schematic of Vema Krishnamurthy active inductor.

Without taking C_{gd} of the transistors into account, the relations of the parameters for this active inductor can be described as:

$$C_p = C_{gs1} \tag{63}$$

$$L_s = \frac{(g_{m1}+g_{m2}+g_{m3})C_{gs3}\left(1+(R_f/g_4)\right)}{g_{m1}g_{m2}g_{m3}+g_{m1}g_{m4}g_3} \tag{64}$$

$$R_s = \frac{g_3(g_{m1}+g_{m2}+g_{m3})}{(g_{m1}g_{m2}g_{m3}+g_{m1}g_{m4}g_3)\left(1+(1/R_f g_4)\right)} \tag{65}$$

From equations (64) and (65), it is very clear that the introduction of R_f increases both L_s and R_s simultaneously. The increased inductance decreases Q factor and also the self-resonant frequency of the inductor. However, the value of inductance is invariant over a large bandwidth as highlighted in (Vema Krishnamurthy et al., 2010).

Such performance degradation can be mitigated by appropriate sizing of M1 and M2, as well as by properly biasing currents I2 and I_b. The proposed structure, implemented in a 0.18-µm CMOS technology, achieved an inductance range of 165–530 nH, a maximum Q-factor of 405, and a self-resonant frequency of 3.8 GHz.

Minaei and Yuce proposed an inverter-based active inductor, as shown in Fig. 3.7 (Minaei & Yuce, 2012). The topology consists of an inverter amplifier connected with two simple transconductors, while one more capacitance C is used to generate the equivalent inductive characteristic. Transistors M1-M6 can be easily biased in the saturation region such that the active inductor operates in a stable and reliable way. The analytical treatment is easily performed because of its structural resemblance to a second-order BPF.

2.7 Minaei-Yuce Active Inductor

Minaei and Yuce proposed an inverter-based active inductor, as illustrated in Fig. 3.7 (Minaei & Yuce, 2012). The topology comprises an inverter amplifier coupled to two basic transconductors, with an additional capacitance C employed to emulate the inductive behavior. Transistors M_1-M_6 can be readily biased in the saturation region, ensuring stable and reliable operation of the active inductor. Due to its structural similarity to a second-order band-pass filter (BPF), the circuit lends itself to straightforward analytical treatment.

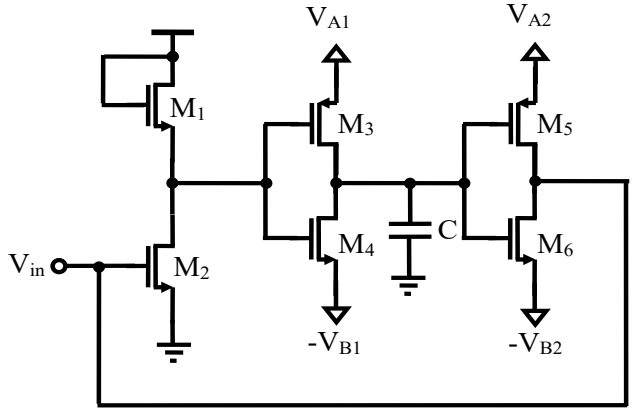


Fig. 3.7 Schematic of Minaei-Yuce active inductor.

2.8 Zhong Active Inductor

Fig. 3.8 shows the schematic of the active inductor proposed by Zhong et al, implemented using the nullator-norator technique (Zhong et al., 2016). The structure is formed by transistors M1, M2, M3, and M4 implementing respectively the transconductances g_{m1}, g_{m2}, g_{m3}, and g_{m4}, while transistor M5 provides bias current to the circuit. The input admittance looking into the input port is given by:

$$Y_{in}=s\left(C_{gs1}+C_{ds4}\right)+g_{o4}+\frac{g_{m1}g_{m3}g_{m4}\left(g_{o3}+g_{o5}\right)}{g_{m2}g_{o3}g_{o5}}\frac{1}{1+s\frac{\left(C_{gs2}+C_{gs3}+C_{ds2}+C_{ds1}\right)}{g_{m2}}}\cdot\frac{1}{1+sC_0\left(\frac{g_{o3}+g_{o5}}{g_{o3}g_{o5}}\right)} \tag{66}$$

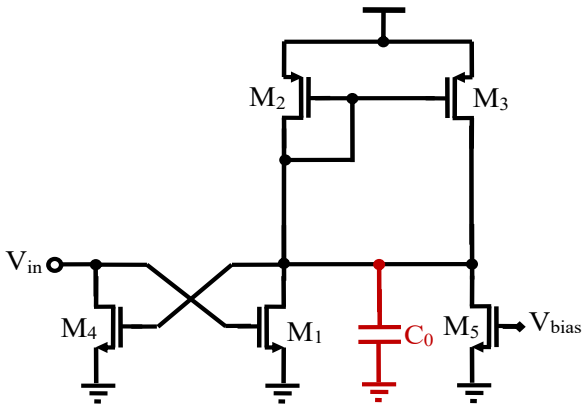


Fig. 3.8 Schematic of Zhong active inductor.

In most practical designs, ω_0 is a high-frequency pole that can be neglected. Equation (66) thus reveals that the inductance behavior can be approximated by either of the two RLC equivalent models depicted in Fig. 3.9.

For high-frequency operation, $\omega > 10\ \omega_1$, equivalent parameters are given by:

$$L_s=C_0\frac{g_{m2}}{g_{m1}g_{m3}g_{m4}} \tag{67}$$

$$R_p=\frac{1}{g_{o4}} \tag{68}$$

$$C_p=C_{gs1}+C_{ds4} \tag{69}$$

At low-frequency operation ($\omega < 10\cdot\omega 1$), the equivalent parameters are:

$$L_s=C_0\frac{g_{m2}}{g_{m1}g_{m3}g_{m4}} \tag{70}$$

$$R_p=\frac{1}{g_{o4}} \tag{71}$$

$$R_s = \frac{g_{m1}g_{m3}g_{m4}\left(g_{o3}+g_{o5}\right)}{g_{m2}g_{o3}g_{o5}} \tag{72}$$

Equations (67) and (70) give a constant inductance at both low and high-frequency limits. Equations (69) and (72), however, yield an operating range dependent upon the parallel capacitance C_p at high frequencies and on the series resistance R_s at low frequencies.

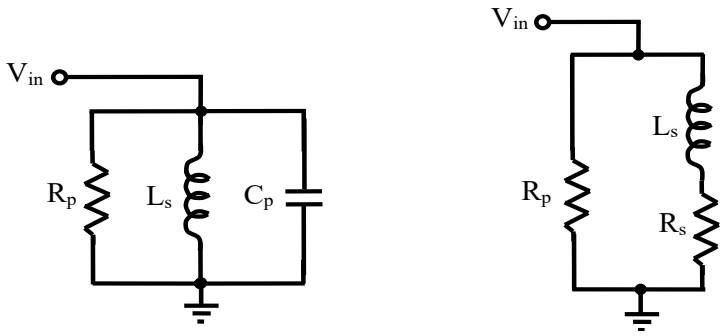


Fig. 3.9 Equivalent RLC Zhong's inductor circuit at: (a) high frequency, and (b) low frequency.

The SRF in both cases is given by the formula below:

$$\omega_0 = \frac{1}{\sqrt{L_s C_p}} = \frac{1}{\sqrt{\frac{g_{m2}}{g_{m1}g_{m3}g_{m4}} C_0\left(C_{gs1}+C_{ds4}\right)}} \tag{73}$$

Zero-frequency point or the lower bound of AI's frequency range is defined as:

$$\omega_z = \frac{R_s}{L_s} = \frac{\left(g_{o3}+g_{o5}\right)\left(g_{m1}g_{m3}g_{m4}\right)^2}{g_{o3}g_{o5}g_{m2}^2 C_0} \tag{74}$$

Equations (73) and (74) show that in order to maximize the frequency range, it is necessary to minimize ω_z. This can be achieved by increasing g_{o2}, g_{m2}, or C_0, the first option being preferable since the capacitor C0 can be realized using MOSFET varactors. Increasing C_0 reduces ω_0 and allows inductance tuning without degrading the quality factor.

When the Q-factor is to be evaluated, account is made for the parasitic resistances of the MOSFETs. The Q-factor, depending on which dominates, is given by:

$$Q = \frac{R_p}{\omega L_s} = \frac{g_{m1}g_{m3}g_{m4}}{\omega g_{o4}g_{m2}C_0} \qquad (R_p \text{ dominates}) \tag{75}$$

$$Q=\frac{\omega L_s}{R_s}=\frac{\omega g_{m2}^2 C_0\left(g_{o3}g_{o5}\right)}{\left(g_{o3}+g_{o5}\right)\left(g_{m1}g_{m3}g_{m4}\right)^2} \qquad (R_s \text{ dominates}) \tag{76}$$

It is worth noting that in the case of dominant R_p, increasing g_{m2} should not be pursued in order not to compromise the upper limit of the frequency range.

2.9 Jeong Active Inductor

Another implementation of a loss-compensated active inductor using feedback resistance by Jeong et al. is shown in Fig. 3.10 (Jeong et al., 2012). The feedback network consists of a resistor R_f connected between the drain of transistor M1 and gate of transistor M2 that has conventionally served to enhance the quality factor of the active inductor. An auxiliary capacitor C_a is added between transistor M1 and the feedback resistor R_f to compensate further for the losses, especially in the subthreshold operation of the active inductor.

Assuming transistors M_n and M_p are ideal biasing current source devices and that $C_{gs} >> C_{gd}$, the input admittance of the active inductor can be expressed as:

$$Y_{in}=sC_{gs1}+g_{ds2}+\frac{\left(sC_{gs2}+g_{m2}\right)\left(sC_a+g_{m1}+g_{ds1}\right)}{sC_{gs2}+\left(g_{ds1}+sC_a\right)\left(1+sC_{gs2}R_f\right)} \tag{77}$$

From equation (77), the RLC parameters of the active inductor are computed as:

$$C_p = C_{gs1}+\frac{C_aC_{gs2}\left(1+g_{ds2}R_f\right)}{C_a+C_{gs2}\left(1+g_{ds1}R_f\right)} \tag{78}$$

$$G_p=\frac{1}{R_p} = g_{ds2}+\frac{C_ag_{m2}+C_{gs1}g_{ds1}+C_{gs2}\left(g_{m1}+g_{ds1}\right)-\omega^2C_aC_{gs1}C_{gs2}R_f}{C_a+C_{gs2}\left(1+g_{ds1}R_f\right)} \tag{79}$$

$$R_s = \frac{g_{ds1}-\omega^2C_aC_{gs2}R_f}{g_{m2}\left(g_{m1}+g_{ds1}\right)} \tag{80}$$

$$L_s = \frac{C_a+C_{gs2}\left(1+g_{ds1}R_f\right)}{g_{m2}\left(g_{m1}+g_{ds1}\right)} \tag{81}$$

Equations (80) and (81) show that the addition of C_a decreases the series resistance Rs while increasing the inductance L_s at the same time. In addition, equation (81) also shows that the inductance can be tuned more linearly than in the conventional Hsiao topology (Hsiao et al., 2002).

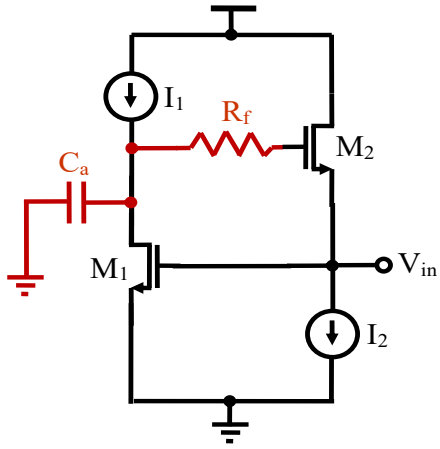


Fig. 3.10 Simplified schematic of Ghadiri-Moez active inductor.

The self-resonant frequency of the Jeong active inductor is slightly reduced relative to the basic configuration, i.e., the simplest gyrator-C based AI, due to the increase in inductance L_s. For the basic case where $R_f = 0$ and $C_a = 0$, the above relationships simplify to:

The self-resonant frequency of the Jeong active inductor is slightly reduced relative to the basic configuration (i.e., the simplest gyrator-C based AI) due to the increase in inductance L_s. For the basic case where R_f=0 and C_a=0, the above relationships simplify to:

$$C_p = C_{gs1}, \qquad R_p = \frac{1}{g_{m1}}, \qquad R_s = \frac{g_{o1}g_{o2}}{g_{m1}g_{m2}} \text{ and } \qquad L_s = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{82}$$

2.10 Reja Active Inductor

Figure 3.11 is the schematic of the active inductor proposed by Reja et al. (Reja et al., 2008; Reja et al., 2010). It is based on the cascode active inductor but includes minor modifications from (Thanachayanont & Payne, 1996). In this topology, a pair of cross-coupled PMOS transistors, M1 and M2, forms a negative impedance circuit that provides positive feedback, allowing inductive behavior to be emulated using capacitive components.

One of the key advantages of this structure is that the currents in all transistors are controlled by a single bias source, the DC bias current I_{DC}. Referring to the schematic, the drain currents of M1 and M3 are directly supplied by I_{DC}, while the drain currents of M2 and M4 are determined by the gate–source voltage V_{gs2} of M2. Because $V_{gs2} = V_b -$

V_{gs3}, transistor M3 can enter the triode region unless the condition $V_b > V_{gs2} + V_{gs3}$ is satisfied.

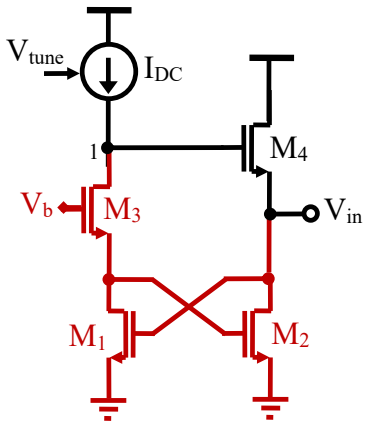


Fig. 3.11 Simplified schematic of Reja active inductor.

Neglecting C_{gd} and g_{ds}, the following relationships can be written:

$$L_s = \frac{C_{gs3}+C_{gs4}}{g_{m1}\left(g_{m3}-g_{m4}\right)}, \qquad R_s = \frac{C_{gs3}+C_{gs4}}{g_{m3}C_{gs1}}, \qquad \text{and} \qquad C_p = C_{gs1} \tag{83}$$

$$\omega_0 = \sqrt{\frac{g_{m1}\left(g_{m3}-g_{m4}\right)}{C_{gs1}\left(C_{gs3}-C_{gs4}\right)}} \qquad \text{and} \qquad Q = \frac{\omega_0\left(C_{gs3}+C_{gs4}\right)}{g_{m3}} \tag{84}$$

These relations indicate that the topology is simple to control, and the Q-factor remains nearly constant since it primarily depends on the self-resonant frequency. To maintain a positive inductance ($L_s > 0$), the condition $g_{m3} > g_{m4}$ must hold.

The proposed active inductor was realized in STMicroelectronics 90-nm digital CMOS technology and simulated in the Cadence SpectreRF® environment (Reja et al., 2008). It was later fabricated and validated in an Ultra Wide Band (UWB) Low-Noise Amplifier (LNA). A similar structure without the cascode transistor was reported by Mehra et al. (2015).

2.11 Manjula-Malarvizhi Active Inductor

Figure 3.12 shows the active inductor proposed by Manjula-Malarvizhi (Manjula & Malarvizhi, 2018). This design merges a cascode configuration with a differential structure. Here, the positive transconductor is realized using an NMOS differential pair (M1 and M2) connected between nodes 1 and 3, while the negative transconductor is implemented as a PMOS cascode stage using transistors M3 and M4. An additional NMOS transistor (M5) is inserted between the two transconductors to improve loss compensation and enhance circuit performance.

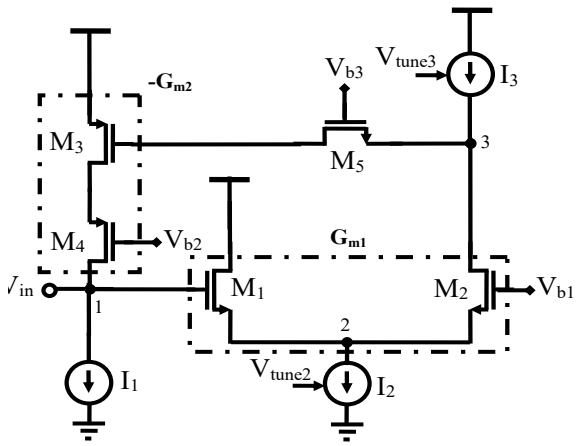


Fig. 3.12 Simplified schematic of Manjula-Malarvizhi active inductor.

The feedback–resistor–cascode–differential configuration of the gyrator–C active inductor provides several advantages:

- Reduced noise sensitivity due to the differential structure.
- Improved Q-factor through the use of a feedback active resistor that reduces the series resistance (R_s).
- A negative R_s generated at the input terminal via the cascode stage, effectively compensating for parasitic losses.
- An extended frequency range achieved through lowering the lower cut-off frequency, resulting in a higher resonance frequency (cascode effect).
- Increased inductive bandwidth owing to the cascode configuration.

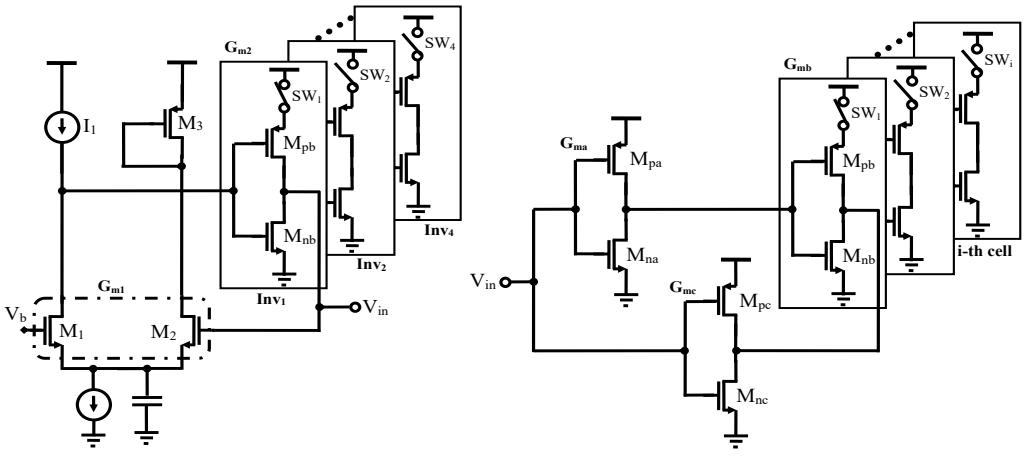
The equivalent inductance can be expressed as:

$$L_s = \frac{g_{o4} g_{o5} C_{gs3}}{g_{m1} g_{m2} g_{m3} g_{m4} g_{m5}} \tag{85}$$

Although the Manjula-Malarvizhi structure achieves better noise immunity, extended bandwidth, and a higher Q-factor, it introduces design challenges. The biasing of both PMOS cascode and NMOS differential transconductors must be carefully tuned to ensure proper operation across the target frequency range. Any mismatch between differential branches can degrade noise suppression, and incorrect biasing may drive the cascode devices out of saturation, diminishing inductive behavior. Furthermore, the inclusion of the additional NMOS transistor (M5) for R_s reduction adds parasitic capacitances, which must be managed carefully to prevent narrowing of the inductive bandwidth.

2.12 Ghorbel Active Inductor

One of the first single-varactor-free topology active inductor implementations relies on a gyrator–C topology using a CMOS process, providing compact area, high power efficiency, and design flexibility. The proposed topology by Ghorbel et al., and seen in Fig. 3.13(a), is based on two transconductance stages: one, G_{m1}, implemented using a differential pair (M1, M2), and the other, g_{m2}, using a bank of CMOS controllable inverters (Inv_1–Inv_4) (Ghorbel et al., 2014; Ghorbel et al., 2015; Haddad et al., 2017; Haddad et al., 2018). Each inverter uses complementary MOS switches (PMOS and NMOS) controlled by a tuning voltage V_{ctrl}, in such a way that by controlling it, the effective transconductance is tuned, which in turn tunes the inductive value. This clearly presents a simple way to provide tunability without using varactors, while maintaining compactness and low power dissipation.



(a) (b)

Fig. 3.13 Schematic of: (a) Ghorbel active inductor, and (b) Slimane active inductor.

Building upon this principle, more sophisticated topologies such as those proposed by Slimane et al. allowed for greater flexibility and finer Q-factor tuning (Slimane et al.

2018). Among these is the push–pull amplifier–based gyrator active inductor shown in Fig. 3.13(b). In this topology, cascaded amplifier cells (Mna-Mpa) and (Mnb-Mpb) implement the positive transconductors, while the amplifier cell (Mnc-Mpc) generates the negative transconductance that provides loss compensation. The capability for multistandard operation is ensured by discrete frequency tuning through a digitally controlled switching operation: multiple (Mnb,Mpb) cells are arranged in parallel, each with a different transconductance, but only one is activated at a time to set the resonant frequency of the inductor over a wide tuning range.

This digitally driven solution not only provides automation for frequency selection but also enables rapid reconfiguration, which is quite suitable for reconfigurable RF front-end systems. However, the introduction of switching transistors brings in new challenges. Noise is introduced through on-resistance thermal contributions, leakage currents in the off state, and flicker noise from both switches and their control circuits. Moreover, charge injection and clock feedthrough during switching events may perturb sensitive analog nodes, possibly up-converting into the RF band through nonlinearities. Proper switch design, low-R_{on} devices, and isolation of digital control paths are consequently of particular importance to preserve the general performance of the active inductor. The Active Inductor was implemented in 0.13µm 1.0V RF CMOS technology and analyzed using Cadence© tools.

2.13 Suresh-Manickam Active Inductor

The MCASFAI, proposed by Suresh-Manickam (Suresh & Manickam, 2020), is an extension of the conventional cascode flipped active inductor (CASFAI) (Thanachayanont & Payne, 1996), basically intended to improve gain and quality factor through enhanced feedback control. In this topology, the core gyrator is implemented by two transistors in a shunt-feedback arrangement, while the inclusion of an auxiliary transistor in the feedback path increases loop gain and loss compensation. The self-resonant frequency is set by the bias current supplied to the gyrator stage, while a separate bias for the auxiliary stage sets its transconductance and, hence, allows precise tuning of the quality factor. By exploiting the intrinsic parasitic capacitance at the input node, the MCASFAI achieves an inductive reactance with higher tunability and improved Q performance compared to the standard CASFAI.

The set of parameters that control the value of RLC-equivalent inductance of the MCASFAI are a bit different compared to the classic CASFAI. Namely, though adding transistors in the feedback path of flipped active inductor improves the quality factor by decreasing the series resistance, inductance is determined basically by the same transconductance and parasitic capacitances of the main device M1. For a fair comparison, for both topologies: inductance and the series resistance are given by:

$$R_s = \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}}, \qquad L_s = \frac{C_{gs2}}{g_{m1}g_{m2}g_{m3}}, \qquad \text{(CASFAI)} \qquad (86)$$

$$R_s = \frac{g_{o2}g_{o3}g_{o4}}{g_{m1}g_{m2}g_{m3}g_{m4}}, \qquad L_s = \frac{C_{gs2}+C_r}{g_{m1}g_{m2}} \qquad \text{(MCASFAI)} \qquad (87)$$

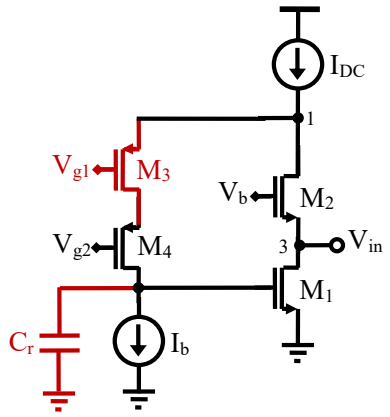


Fig. 3.14 Simplified schematic of Suresh-Manickam active inductor.

2.14 Prameela-Daniel Active Inductor

Fig. 3.15 presents the R_{fb}-DCAI topology proposed by Prameela and Daniel in (Prameela & Daniel, 2020). Here, the transistors M2 and M3 are cascaded with the auxiliary devices M22 and M33 to improve the overall performance. The cascoding arrangement helps in several ways: it increases the output impedance, improves gain, and reduces the series resistive loss considerably; this results in an improved quality factor Q. In addition, the cascoding setup permits the intrinsic conductances g_{o2} and g_{o3}, affecting the equivalent parallel resistance R_p. This is similar to all cascode-based topologies, where Q-enhancement comes with the price of a reduced output voltage swing. Thus, the minimum supply voltage requirement set by the stacked devices is typically no less than three times the overdrive voltage ($3V_{sat}$), a constraint explicitly considered in this design. Therefore, a smaller output swing is a natural trade-off while trying to achieve a higher quality factor by using the cascode configuration.

Transistors M4-M6 in the circuit are used to replace the ideal current sources I2-I4 from the original topology invented by (Yodprasit & Ngarmnil, 2000), thus making it practical. Additionally, the bias voltage V_b provides a method of controlling the effective parallel resistive loss of the active inductor. The self-resonant frequency can be tuned by adjusting the current I1, thus allowing flexibility for frequency optimization.

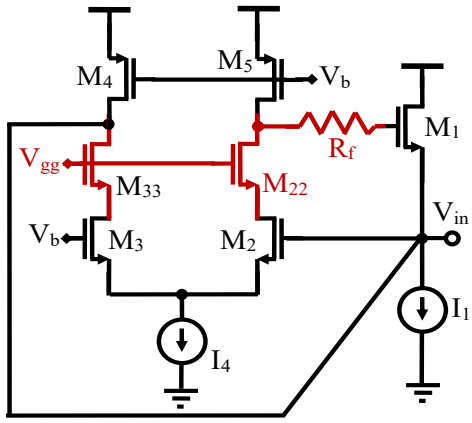


Fig. 3.15 Schematic of Prameela-Daniel active inductor.

2.15 Sabbaghi-Ebrahimi Active Inductor

The conventional current-reused active inductor by Wu et al. (2003) represented in Fig. 3.16(a) is one of the commonly used structures due to its simplicity and low power dissipation. In this structure, the negative and positive transconductances of a gyrator are formed using transistors M1 and M2, respectively. The structure can be treated as an RLC circuit with the following parameters:

$$L_s=\frac{C_{gs1}}{g_{m1}g_{m2}},\quad R_s=\frac{g_{o2}}{g_{m1}g_{m2}},\quad R_p=\frac{1}{g_{o1}+g_{m2}}\approx\frac{1}{g_{m2}}\quad\text{and}\quad C_p=C_{gs2}\qquad(88)$$

Further manipulation of these expressions reveals that the series resistance R_s of the classical current-reused AI is fairly large, which limits the attainable quality factor. To improve this, a topology variation is introduced (Sabbaghi & Ebrahimi, 2021), depicted in Fig. 3.16(b), in which transistors M1 and M2 have been adapted to constitute a flipped voltage follower FVF (Carvajal et al., 2005).

This topology can be represented by an RLC equivalent network with its parameters giver by:

$$L_s=\frac{g_{o3}C_{gs1}+g_{o2}C_{gs2}}{g_{m1}g_{m2}g_{m3}},\quad R_s\approx\frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}},R_p=\frac{1}{g_{o1}+\dfrac{g_{m2}g_{m3}}{g_{o2}+g_{o3}}}\ \text{and}\ C_p=C_{gs3}\qquad(89)$$

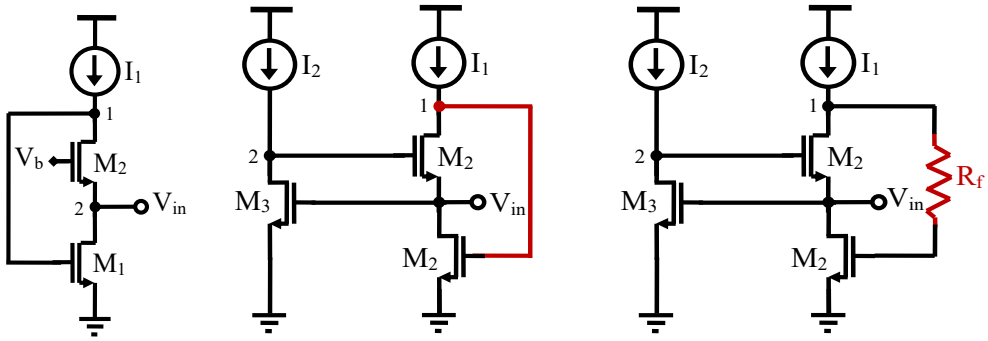
As can be seen, the equivalent series resistance is decreased with respect to its original form. This indicates a considerable enhancement in the Q-factor. Nevertheless, the configuration also increases the parallel conductance while reducing the overall

improvement. For example, based on the assumptions of $g_{o2}=g_{o3}=(r_{o3})\text{-}1$, the equivalent R_s decreases by a factor of $1/(g_{m3}r_{o3})$, but the parallel conductance increases by $1+2g_{m3}r_{o3}$.

To further increase the Q-factor, a feedback resistor R_f can be added, as improved by Sabbaghi and Ebrahimi in (Sabbaghi & Ebrahimi, 2021) and shown in Fig. 3.16(c). In the small-signal analysis of this configuration, the following L_s and R_p parameters are obtained:

$$L_s=\frac{R_f g_{o2}g_{o3}C_{gs1}+g_{o3}C_{gs1}+g_{o2}C_{gs2}}{g_{m1}g_{m2}g_{m3}}, \quad \text{and} \quad R_p=\frac{1}{g_{o1}+\dfrac{g_{m2}g_{m3}}{g_{o2}+g_{o3}+R_f g_{o2}g_{o3}}} \quad (90)$$

It is clear from these expressions that with an increase in Rf, the quality factor increases but at the cost of SRF reduction, hence limiting the bandwidth. Also, the value of inductance is proportional to R_f, which implies higher resistance results in larger inductance but again at the cost of SRF reduction. This trade-off in Q-factor, inductance tuning, and bandwidth represents the central challenge of this improved topology.



(a) (b) (c)

Fig. 3.16 Simplified schematic of current-reused AI: (a) Conventional structure, (b) FVF structure, and (c) FVF with resistance feedback structure.

2.16 Behera Active Inductor

Behera et al. introduce another enhanced active inductor topology, depicted in Fig. 3.17, in which multiple circuit modifications were applied to enhance both the inductance and the Q-factor (Behera et al., 2022). The transistor M7 is stacked below M5 in order to increase the cascode effect, while an added gain stage contributed by M6 increases the total performance. The biasing is performed through the voltages V_{b1} and V_{b2} applied to the sources of M1 and M2, respectively, while the equivalent inductance is set up through the voltage V_t, connected to M8 and M9. Furthermore, M10 together with the R2–C2 branch, replaces the traditional biasing tail current source to keep the resistance

nature. The enhancement is developed in adding the resistor R1 together with M7 and M4 to provide extra inductive resistance that enhances the impedance and, hence, significantly increases the inductance and the Q-factor of the active inductor.

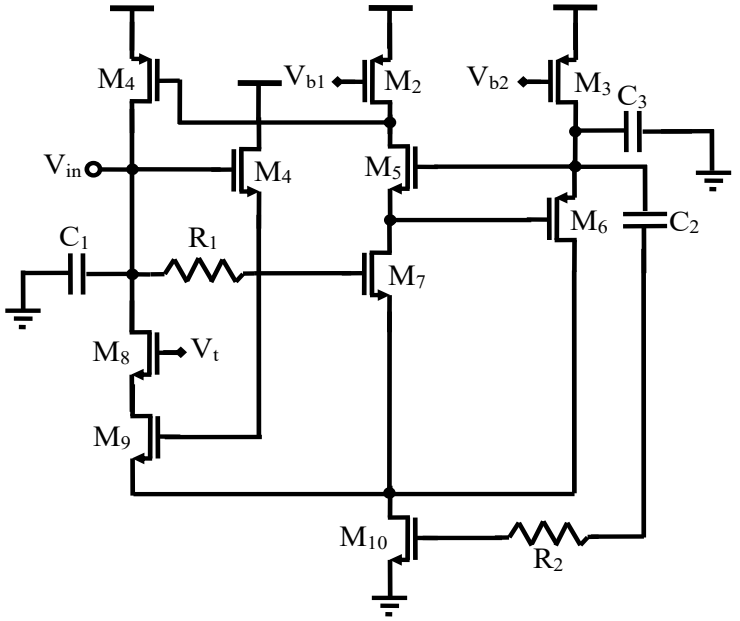


Fig. 3.17 Schematic of Behera active inductor.

The analysis of Behera active inductor is well detailed in (Behera et al., 2022). The structure is fabricated in a 65nm CMOS technology and demonstrated in a VCO for automotive radar applications, where it achieves a maximum Q-factor of 6825.

2.17 Saad Active Inductor

Yet another variant of the RC-feedback-based active inductors is shown in Fig. 3.18. In this implementation, proposed by Saad et al., an RC network is added between the two transconductors to compensate for the intrinsic losses and hence improve the quality factor (Saad et al., 2016). One of the unique points of this technique is that the inductance value and the Q-factor are tunable independently via the effective transconductance of the active devices, which makes it even more attractive for narrowband applications where exact tuning is necessary.

In the topology presented, the negative transconductor is implemented by a common-source transistor (M1), while the positive one is realized as a cascaded differential common-gate stage constituted by transistors M2 and M3. This provides not only stabilization of the operation but also an improvement in the tuning flexibility. The implementation in 90-nm CMOS technology reached an inductance of about 26 nH and

showed the maximum quality factor of 895 at 1.77 GHz, thus proving the efficiency of the RC feedback in enhancing both inductive behavior and performance. This topology will be further explored in the next chapter.

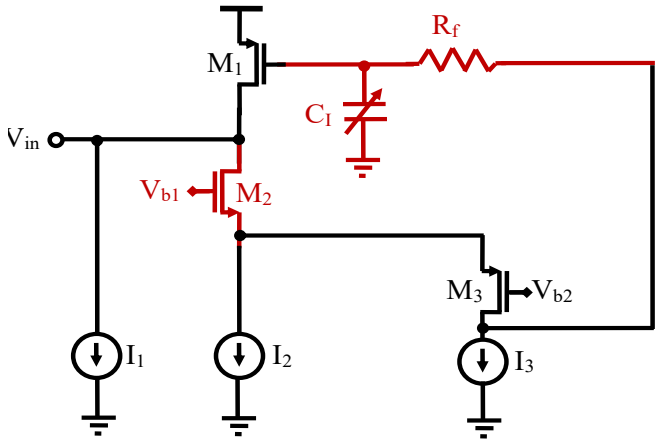


Fig. 3.18 Simplified schematic of Saad active inductor.

Conclusion

A review of single-ended gyrator-C active inductor designs is presented, and steady progress during the last 15 years toward overcoming the various limitations of early implementations is pointed out. From architectural refinements to biasing innovations and parasitic-aware optimizations, active inductors have become increasingly viable for RF and mixed-signal integrations, presenting competitive alternatives to passive inductors in terms of area efficiency, tunability, and performance.

None of the designs simultaneously achieves the highest figure of merits, but taken together, all of these innovations show that major trade-offs can be mitigated through appropriate selection of topology and design approach. Designs from Ghadiri-Moez, Bhattacharya, Lai-Zheng, and more recent proposals, such as those by Saad and Sabbaghi-Ebrahimi represent this evolution, demonstrating how creative use of CMOS device properties and various feedback mechanisms can yield robust, high-Q tunable inductors.

In the future, too, the reconfigurable and adaptive RF front-end trend will further push research in active inductors towards ultra-low-power implementation, compatibility with advanced CMOS nodes, and integrations into highly miniaturized multi-standard systems. Innovations reviewed here further open up the design space of active inductors and point out their crucial role in shaping the future of compact tunable RF circuits.

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