Deep Science Publishing, 2025
https://doi.org/10.70593/978-93-7185-269-2_2

Chapter 2: The Evolutionary Era — Toward the Golden Age of Active Inductors

Hatem Garrab [1,2]

[1] *Electronics and Micro-Electronic Laboratory (LEμE), Bd de l'environnement, Monastir 5000, Tunisia.*
[2] *Higher Institute of Applied Sciences and Technology of Sousse, University of Sousse, Street Taher Ben Achour, 4003 Sousse, Tunisia.*

Abstract: Active inductors (AIs) implemented using gyrator-C configurations have become a cornerstone of radio frequency integrated circuit (RFIC) and analog design, providing wide tunability, small size, and CMOS compatibility compared with their passive spiral counterparts. This chapter is dedicated to the in-depth study of single-ended gyrator-C active inductors, starting from the basic operation principles, parasitic effects, and equivalent impedance modeling of this family of circuits. Several simple configurations are first reviewed, followed by the effective evolution overview and the main performance enhancement techniques developed up to the mid-2000s. Such techniques have included the use of resistive feedback, cascode and regulated cascode topologies, auxiliary capacitors, and advanced biasing schemes, analyzed for their effectiveness in extending inductance tuning, quality factor, frequency range, and power efficiency. At the end, synergistic integration of these techniques to implement High-Q, wideband, and low-loss inductors suitable for RF and microwave applications is emphasized.

Keywords: Active Inductor, Gyrator-C Topology, Radio Frequency Integrated Circuits (RFICs), CMOS RF Design

1 Introduction

The demand for compact, tunable, power-efficient RF integrated circuits has continuously strengthened interest in active inductors as an alternative to the traditional on-chip spiral inductors. Whereas passive inductors are troubled with large silicon area, limited quality factor, and poor tunability, the active implementations based on gyrator-C structures offer electronically controllable inductance within standard CMOS technology that allows a higher integration density and flexible frequency adaptation.

Of all active inductor realizations, the single-ended gyrator-C is the most basic and popular topology investigated. It has an inductive input impedance synthesized by means

of two transconductors and a capacitor whereby device parasitics set a bound on its useful frequency range and quality factor. The basic configuration still suffers from several drawbacks including finite output resistance, parasitic capacitances, noise, and instability that limit its direct application in RF circuits.

In the face of such challenges, significant research in the period between the mid-1990s and 2007 introduced a wide range of enhancement techniques into the literature (Yuan, 2008). Enhancement techniques that include resistive feedback to increase inductance tunability; cascode and regulated cascode architectures to suppress parasitics and extend frequency range; auxiliary capacitors to decouple inductance control from loss mechanisms; and optimized biasing strategies to balance tunability, linearity, and power consumption all feature prominently. More advanced hybrid solutions combine several such techniques to obtain high-performance inductors for oscillator, filter, and impedance-matching networks.

It covers the basic principles, evolution, and techniques for enhancing the performance of single-ended gyrator-C active inductors. Basic configurations and their equivalent models, with discussions on the effects of parasitics on frequency behavior and Q-factor, are introduced in Section 2. Section 3 describes important methods for enhancing performance: resistive feedback, cascode architectures, biasing schemes, and low-voltage implementations among them. Section 4 highlights synergistic integrations that have taken place in advanced designs. The key issues are summarized at the end of the chapter, and there is further discussion of the main insights with respect to their value in contemporary RF circuit applications.

2 Basic Single-Ended Gyrator-C Active Inductor

2.1 Simplest Configuration of Gyrator-C Based Active Inductor

The transconductors of gyrator-C networks can be configured in several ways. The fundamental combination of transconductors is implemented as a common-source transconductor g_{m-}, with common-drain (CD) or common-gate (CG) transconductor g_{m+}, as depicted in Fig. 2.1 and Fig. 2.2. Notice that the differential-pair transconductors possess a positive transconductance g_{m+}.

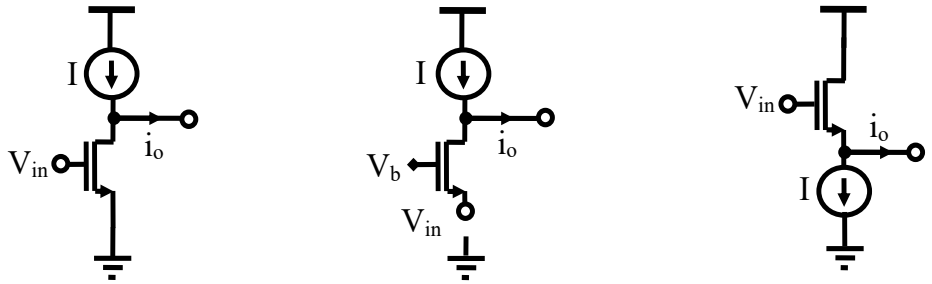
- In a standard CMOS implementation, the first and second transconductance stages are realized using common-source (CS) MOSFETs along with a positive transducer, depending on whether it is a single-ended or differential implementation. A simple single-ended realization is shown in Fig. 2.3 where:

- Transistor M1 (NMOS): Serves as the voltage-to-current converter with transconductance g_{m1}.
- Transistor M2 (NMOS or PMOS): Acts as the current-to-voltage converter with transconductance g_{m2}.

Bias current sources: Supply the current needed by M1 and M2 to operate in the saturation region and thereby set g_{m1} and g_{m2}.

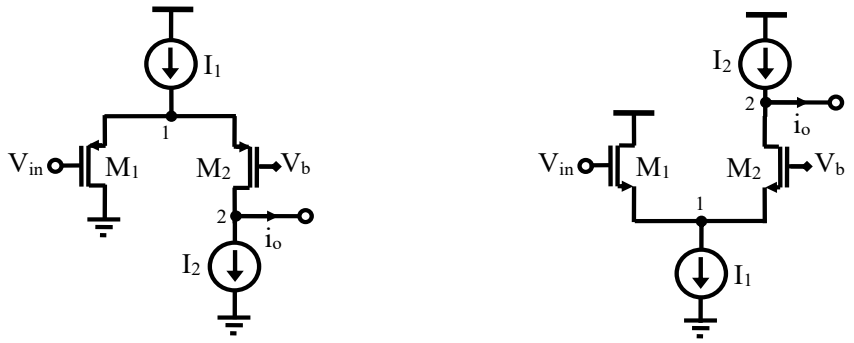
In practical implementations, the active inductor behavior is made non-ideal due to parasitic elements contributed by the MOSFETs and interconnects. These include:

- Output conductance g_{o1}, g_{o2}, which add parallel resistive paths to the transconductance stages.
- Parasitic capacitance C_p, due to the MOSFET gate-drain and drain-bulk capacitances.
- Series resistance R_s: This represents the channel resistance and interconnect losses.



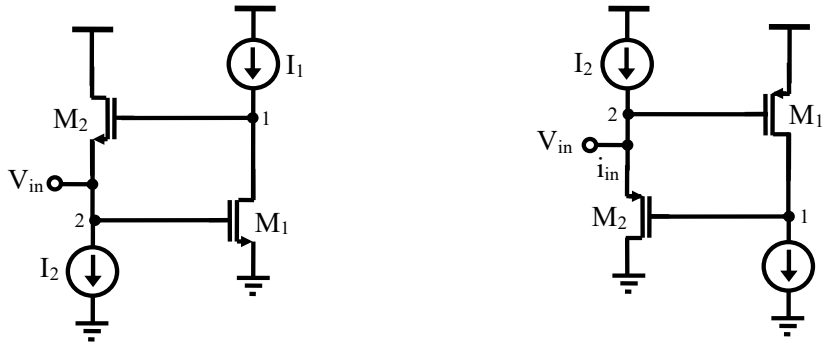
(a) (b) (c)

Fig. 2.1 Schematic of basic transconductor: (a) common source, (b) common gate, (c) common drain.



(a) (b)

Fig. 2.2 Schematic of basic transconductor: (a) and (b) examples of differential-pair transconductors.



(a) (b)

Fig. 2.3 Schematic of basic active inductor: (a) CS-CD: only NMOS, and (b) CS-CD: only PMOS, topology.

The input impedance, when including these parasitics, is:

$$Z_{in} = \frac{sL_s + R_s}{1 + sR_pC_p} \tag{28}$$

where:

$$L_s = \frac{C_{gs2}}{g_{m1}g_{m2}} \text{ is the equivalent inductance.} \tag{29}$$

$$R_s = \frac{g_{o1}}{g_{m1}g_{m2}} \text{ models series loss.} \quad . \tag{30}$$

$$R_p = \frac{1}{g_{m1}} \text{ represents parallel resistance.} \tag{31}$$

$$C_p = C_{gs1} \text{ is the total parasitic capacitance at the input-node} \tag{32}$$

The circuit is inductive over a certain range of frequency. For low frequencies, impedance increases linearly with frequency due to the inductor-like behavior. At high frequencies, the parasitic capacitance C_p provides self-resonant frequency given by:

$$\omega_0 = \frac{1}{\sqrt{L_sC_p}} = \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}} \tag{33}$$

Above this frequency the impedance becomes capacitive and the inductor emulation breaks down. This bounds the upper limit of the useful frequency ranges for the active inductor

The zero frequency of inductive behavior is given by:

$$\omega_z = \frac{R_s}{L_s} = \frac{g_{o1}}{C_{gs2}} \tag{34}$$

The pole frequency, where capacitive parasitics are dominant:

$$\omega_p = \frac{1}{R_p C_p} = \frac{g_{o2}}{C_{gs1}} \tag{35}$$

The inductive behavior is valid in the range:

$$\omega_z < \omega < \omega_p \tag{36}$$

The following simplified expression gives a good approximation of the quality factor Q of the gyrator–C active inductor at low frequencies:

$$Q = \frac{\omega L_s}{R_s} \tag{37}$$

This equation holds good if the parasitic capacitance and all other high-frequency effects are negligible. But when the applied frequency is near the self-resonant frequency, all the parasitic elements start affecting Q. The additional parallel capacitance C_p and the parallel resistance R_p introduce complexities in the Q-factor calculation due to MOSFET parasitics, such as gate-drain capacitance and finite output conductance, respectively.

In deep-submicron CMOS technologies, the output conductance of transistors is small compared with their transconductance. In this situation, the value of R_p becomes highly dominant. As the frequency increases toward resonance, the Q-factor of the circuit becomes increasingly dominated by R_p, rather than R_s. In such a regime, quality factor is no longer limited by series resistance itself but due to the parallel resistance and capacitive parasitics. Near resonance, Q can be approximated by:

$$Q(\omega_0) \approx \frac{R_s}{\omega L_s} \approx \sqrt{\frac{C_{gs1} g_{m2}}{g_{m1} C_{gs2}}} \tag{38}$$

2.2 Other Simplest Configuration of Gyrator-C Based Active Inductor

Two other sets of fundamental topologies have also been proposed in the literature, offering alternative ways of realizing gyrator–C active inductors. Fig. 2.4 shows possible gyrator–C structures presented in the literature (Thanachayanont et al., 2002; Yuan, 2007).

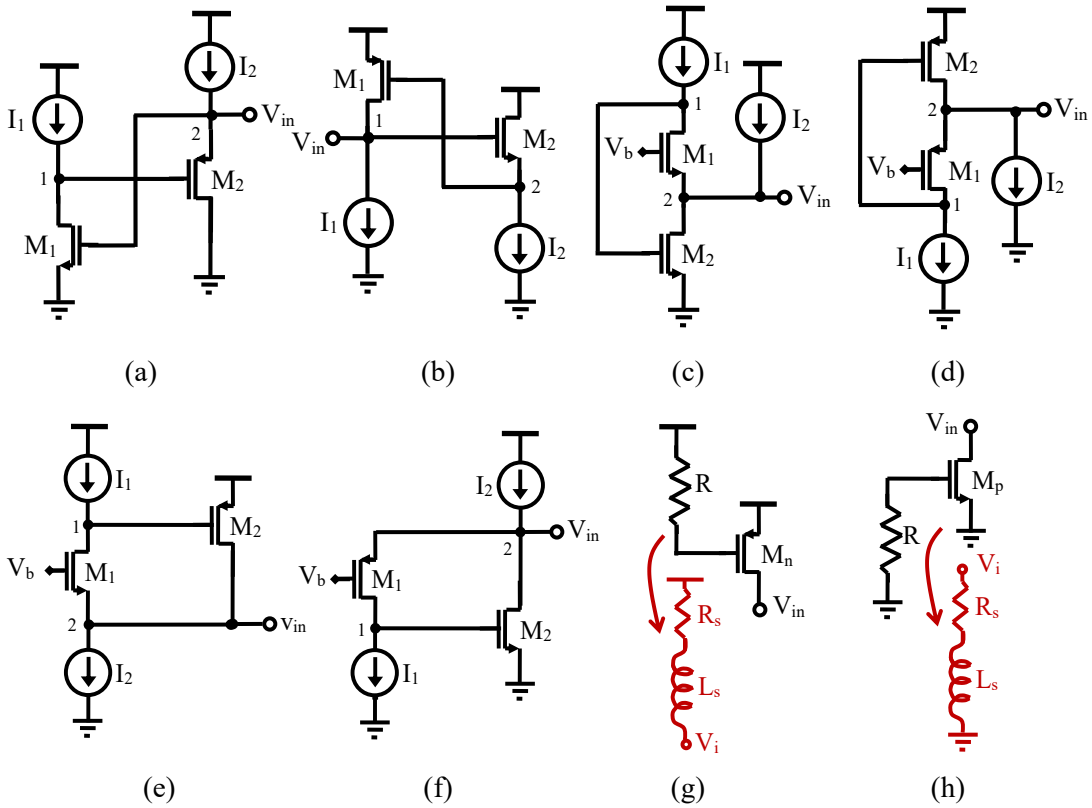


Fig. 2.4 Possible simplified schematics of basic gyrator-C AI: (a) CS-CD: NMOS-PMOS, (b) CS-CD: PMOS-NMOS, (c) CG-CS: NMOS only, (d) CG-CS: PMOS only, (e) CG-CS: NMOS-PMOS, (f) CG-CS: PMOS-NMOS, (g) single PMOS, and (h) single NMOS.

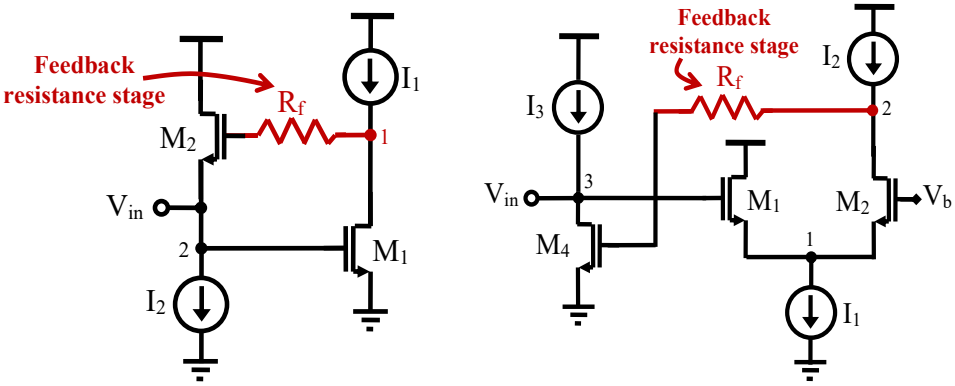
3 Evolution of Single-Ended Gyrator–C Active Inductor Designs: Performance Improvement Strategies (Up to Year 2007)

Since the emergence of the first single-ended gyrator–C active inductor, many improvements have been proposed to overcome the intrinsic bounds on its Q-factor, linearity, noise, tunability, and stability. In fact, from the mid-1990s until 2007, the research community has pursued a large number of architectural changes and circuit techniques aimed at practical active inductor usability in both RF and analog applications. The following section offers a perspective into the evolution of the single-ended gyrator–C topologies while highlighting the most meaningful approaches developed to achieve an advance in performance. Also, it will look at their widespread reuse and adaptation throughout the years by subsequent research, where these same techniques have enabled performance enhancements effectively, with a minimum of modifications, and thus demonstrating the lasting power of those techniques in the

design of analog integrated circuits. These include innovations such as feedback resistance techniques, cascode structures, source degeneration, and biasing schemes, which form the foundation for many of today's active inductor architectures.

3.1 Feedback Resistance Configuration of Gyrator-C Based Active Inductor

The addition of a feedback resistor R_f between the two transconductance stages is an effective technique to enhance the performance of gyrator–C active inductors. This technique modifies the basic structure of the lossy single-ended gyrator–C circuit, its transforms its impedance characteristics and can provide superior design flexibility. The introduction of R_f in the feedback path makes the active inductor simultaneously enhance the inductance value, quality factor, and tunability, at the cost of bandwidth reduction. Fig. 2.5 exhibits two examples of possible implementation using a feedback resistance (Szczepkowski et al., 2007; Abdalla et al., 2006).



(a) (b)

Fig. 2.5 (a-b) Example of gyrator-C active inductor using a feedback resistor R_f.

The impact of R_f on the equivalent inductance is direct. The expression for modified inductance becomes:

$$L_{s\text{-feedback}} = \left(1+\frac{1+g_{o1}R_f}{1+sC_{gs1}R_f}\right)\times\frac{C_{gs1}}{g_{m1}g_{m2}} \tag{39}$$

This simplifies, at low frequencies $sC\,R_f \ll 1$, to:

$$L_{s\text{-feedback}} \approx \left(1+g_{o1}R_f\right)\times\frac{C_{gs1}}{g_{m1}g_{m2}} \tag{40}$$

This equation indicates that inductance is linearly increased with the increase of R_f. In practice, tuning R_f allows the designer to set the magnitude of inductance without having

to change the capacitor C_{gs1} or the transconductance stages. This property significantly enhances inductance tunability, which is particularly useful for applications where wideband or adaptive frequency control is needed.

Many types of tunable R_f have been proposed to extend the flexibility in design:

- There are designs where R_f is implemented by a PMOS transistor biased in the triode region. Here, the gate voltage controls channel resistance. The effective feedback resistance may also be dynamically tuned by varying the gate bias, thus enabling continuous inductance tunability (Hammadi et al., 2014; Hammadi et al., 2017; Saad et al. 2025).
- Alternative implementations also use a passive resistor in parallel or in series with an NMOS transistor operating in the triode region. The NMOS resistance is controlled by the gate-source voltage V_{tune} and thus, for all practical purposes, modifies Rf. As V_{tune} increases, NMOS resistance decreases, thereby decreasing the overall inductance and thus giving a voltage-controlled tunability easily as done by Wei et al. (2005), Mukhopadhyay et al. (2005), Ler et al. (2009), and Pakasiri et al. (2024).
- In digitally controlled systems, R_f can be implemented using discrete resistors selected by a multiplexer, thus enabling binary-coded inductance control. For instance, a 2-bit control word may select among four different resistances for allowing multiband operation in VCOs or tunable filters (Wu et al., 2007).

3.2 Cascode Architectures Used in Gyrator-C Based Active Inductor

One of the major developments in gyrator–C active inductor design is the introduction of cascode architectures. The cascode configuration remedies a number of serious deficiencies in the basic single-ended gyrator–C topology, specifically with regard to parasitic capacitance control, Q-enhancement, linearity, and high-frequency operation.

In the simple gyrator–C circuit, the transconductance stages have a finite intrinsic output resistance due to channel-length modulation in the MOSFETs that limits the output impedance. Consequently, the output node sees a lower parallel resistance R_p, which reduces the quality factor at high frequencies and increases the sensitivity of the circuit to parasitic capacitances. The Miller effect represented by the gate–drain capacitance C_{gd} aggravates bandwidth limitations by introducing unwanted poles and further narrowing the useful frequency range for inductive behavior.

The cascode configuration shown in this example from Fig. 2.6 remedies these problems by stacking an additional MOSFET, which acts as a common-gate buffer, on top of the transconductance transistor (Thanachayanont & Payne, 1996; Ghen et al., 2002; Li et al., 2011; Saberkari et al., 2014; Saberkari et al., 2016). The output impedance of the

transconductance stage significantly increases with this structure, effectively boosting R_p and improving the Q-factor of the whole circuit, particularly when the self-resonant frequency is approached where energy loss is dominated by R_p.

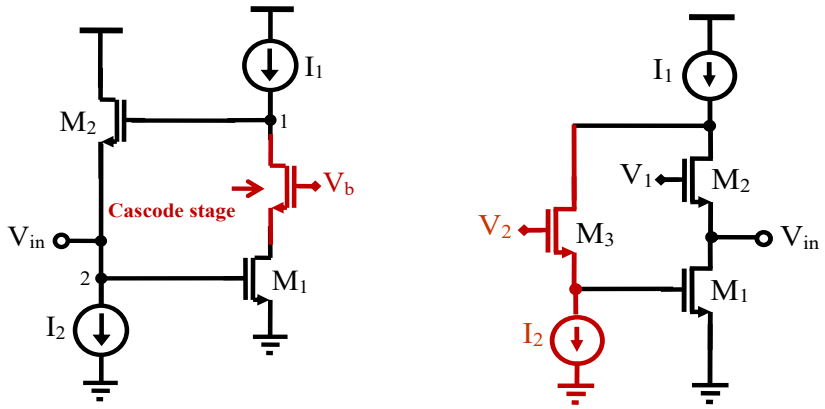


Fig. 2.6 Examples of gyrator-C active inductor using a conventional cascode stage, (a) Basic AI (Thanachayanont & Payne, 1996; Ghen et al., 2002), and (b) Flipped AI (Li et al., 2011; Saberkari et al., 2014 Saberkari et al., 2016).

The regulated cascode (RGC) is an enhancement as opposed to the basic cascode, which was first introduced to increase the output impedance and bandwidth without excessively increasing the voltage headroom requirements. In an RGC configuration, a local feedback is utilized to control the voltage at the intermediate node (the drain of the transconductance transistor), effectively keeping it constant and suppressing variations due to input signals (Sackinger & Guggenbuhl, 2002; Wang & Wang, 2012). Fig. 2.7 presents an example of implementation of a gyrator-C AI using a regulated cascode stage.

This is typically implemented by:

- Adding a transconductance amplifier or voltage buffer that senses the voltage at the drain of the active device and adjusts the gate of the cascode transistor to keep the drain voltage constant.
- Passive regulation: By employing current mirrors or auxiliary amplifiers to perform the regulation without adding significant power consumption.
- The multi-regulated cascode (MRGC) further extends the RGC concept and introduces multi-level regulation across different nodes within the circuit, as demonstrated in Fig. 2.7 (Manetakis et al., 1996).

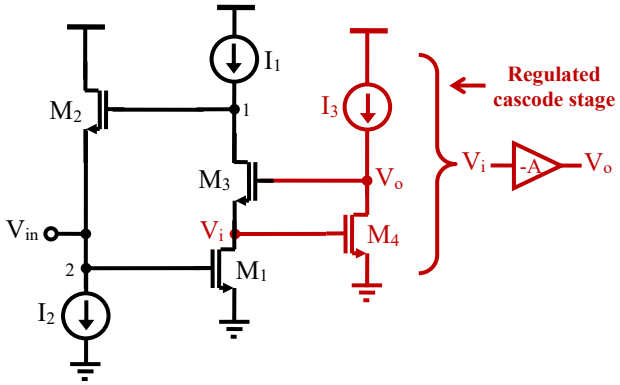


Fig. 2.7 Example of gyrator-C active inductor using a regulated cascode stage.

The goal is to further enhance:

- Output impedance, by cascading multiple RGC stages.
- Impedance linearity: all nodes that lie in between remain at the same voltages, independent of variations in signals.
- High-frequency stability: by preventing unwanted feedback loops through parasitic paths.

In MRGC designs, each cascode stage contains an independent local feedback loop. The local feedback loops are usually provided by auxiliary amplifiers or voltage followers as shown in Fig. 2.8. This topology drastically enhances broadband performance and noise immunity, especially in low-voltage deep-submicron CMOS processes for which supply voltages have been dramatically reduced.

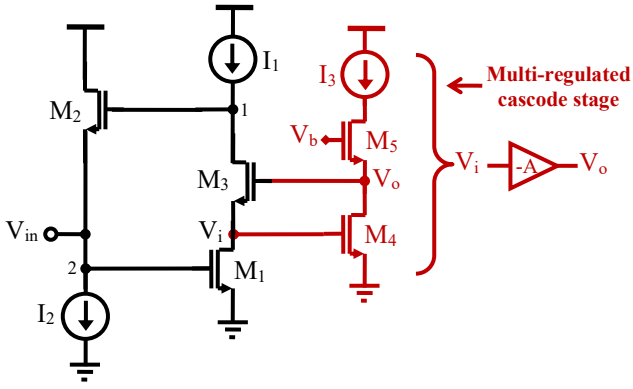


Fig. 2.8 Example of gyrator-C active inductor using a multi-regulated cascode stage.

Table 2.1 gives a comparison of the output conductance and the minimum supply voltage among basic, cascode, regulated cascode, and multi-regulated cascode topologies.

Table. 2.1 Comparison of output conductance minimum supply voltage and in basic and cascode transconductor configurations.

Transconductor type	Output impedance (G_o)	Minimum supply V_{DD}
Basic gyrator-C AI	$G_o = \frac{1}{r_o}$	$2V_{sat}$
Cascode gyrator-C AI	$G_o = \frac{1}{r_o\left(r_{o2}g_{m2}\right)}$	$3V_{sat}$
Regulated cascode gyrator-C AI	$G_o = \frac{1}{r_o\left(r_{o2}g_{m2}\right)\left(r_{o3}g_{m3}\right)}$	$V_{sat}+2V_{TH}$
Multi-regulated cascode gyrator-C AI	$G_o = \frac{1}{r_o\left(r_{o2}g_{m2}\right)\left(r_{o3}g_{m3}\right)\left(r_{o4}g_{m4}\right)}$	$V_{sat}+2V_{TH}$

3.3 Auxiliary Capacitor Used in Gyrator-C Based Active Inductor

A practical realization of the gyrator–C active inductor architecture includes an additional capacitor in the feedback path between the transconductance stages, as shown in Fig. 2.9(a) (Karsilayan & Schaumann, 2000; Xiao & Schaumann, 2002; Xiao & Schaumann, 2004) and Fig. 2.9(b) (Uyanik & Tarim, 2007; Momen et al., 2016).

Including this capacitor offers an effective means of decoupling the inductance control from parasitic resistive losses, allowing independent optimization of critical performance parameters. The equivalent inductances observed in Fig. 2.9 are expressed as:

$$L_s = \frac{C_{gs2}+C}{g_{m1}g_{m2}\dfrac{g_{m4}}{g_{m3}}} \quad \text{(a)} \qquad (41)$$

$$L_s = \frac{C_{gs3}+C_I}{g_m g_{m3}} \quad \text{(b)} \qquad (42)$$

By appropriately selecting the shunt capacitance, the equivalent inductance L_s can be increased without proportionally increasing the series resistance R_s, thereby enhancing the quality factor Q across the desired frequency range. Along with inductance tuning, the shunt capacitor improves circuit stability by reducing high-frequency gain peaking and mitigating the effects of device parasitics. This approach is especially advantageous in deep-submicron CMOS processes, where parasitic capacitances can be exploited rather than minimized.

For tunable designs, the additional capacitance may be implemented using varactors (Ghorbel et al., 2011; Momen et al., 2016; Ebrahimi & Shaterian, 2024) or MIM/MOM capacitor networks (Saad et al., 2016), enabling post-fabrication tuning of L_s, the resonant frequency f_0, and Q through simple bias control. Thus, the shunt capacitor method offers a compact, CMOS-compatible, and flexible approach for improving gyrator–C active inductors, complementing other techniques such as cascode biasing and resistive feedback.

3.4 Biasing schemes to improve active inductor performance

The biasing strategy is critical in the gyrator-C active inductor to set the inductance, quality factor (Q), noise characteristics, and power consumption. In addition to merely setting the operating point of the MOSFETs or OTAs, biasing schemes can be engineered to reinforce desired metrics while minimizing non-idealities.

The widely used method is current bias tuning, where the transconductance stage bias current is adjusted to vary the effective transconductance gm. Increasing gm normally reduces R_s, improving Q-factor. This does come, however, at a cost of higher power consumption and potential stability degradation. CMOS implementations often use programmable current mirrors or digitally controlled bias DACs for accurate tuning.

Adaptive biasing allows for further optimization by dynamically changing the bias current based on either the amplitude of the input signal or the operation frequency as shown in Li et al. (2011). This permits the inductor to have a high Q-factor within the desired band while power is saved during idle conditions. This approach proves to be particularly effective in RF transceivers used for IoT and mobile devices where power efficiency becomes indispensable.

Cascode biasing has often been adopted in high-frequency applications to diminish parasitic capacitance effects and enhance node isolation, such that higher resonant frequencies f_0 and improved linearity can be achieved (Weng & Kuo, 2007; DiClemente & Yuan, 2007) as shown in Fig. 2.10. Cascode biasing is usually united with regulated cascode (RGC) configurations for even higher output resistance and less g_{ds}-related losses.

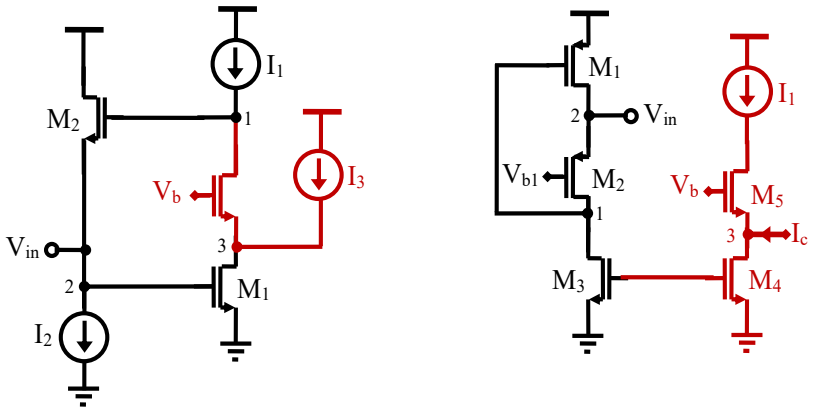
Multi-bias networks can also be used to enable independent tuning of each transconductance stage in differential or floating gyrator–C topologies. Thus, it offers greater freedom in the control of L_s and Q with added flexibility for optimization of noise and linearity.

Biasing schemes in general represent a very effective yet low-overhead means of fine-tuning active inductor performance. When well designed, they can significantly increase tunability, reduce losses, and improve RF behavior without extra area. Table 2.2

summarizes the main biasing methods, highlighting their advantages, trade-offs, and best use cases.

Table. 2.2 Summary of biasing schemes for gyrator–C active inductors.

Biasing technique	Main advantage	Trade-offs	Best-use cases
Current bias tuning	Simple control of g_m to adjust L_s and improve Q	Higher bias current increases power consumption; possible stability issues	Fixed-frequency RF front-ends with fine Q control
Adaptive tuning	Dynamic power saving; maintains high Q in-band	More complex control circuitry required	Low-power, burst-mode IoT and mobile systems
Cascode biasing	Suppresses parasitic effects; improves high-frequency performance	Slightly higher voltage headroom requirement	High-f_0 designs, low-parasitic CMOS AIs
Regulated cascode biasing	Maximizes output resistance; reduces g_{ds}-related losses	More bias circuitry; increased complexity	Low-noise, high-Q active inductors
Multi-bias networks	Independent tuning of multiple stages; greater flexibility	Requires additional bias lines and control logic	Differential or floating AI topologies with fine-tuned L and Q



(a) (b)

Fig. 2.10 A modified gyrator–C-based AIs with: (a) current-reuse cascode stage proposed by Weng & Kuo (2007), and (b) replica biasing proosed by DiClemente & Yuan (2007).

A low-voltage active inductor represents another solution for power-efficient designs. The topology proposed by Ngow-Thanachayanont (Sae-Ngow & Thanachayanont, 2003) introduces an additional branch to address biasing issues typical of Lin–Payne inductors. The improvement uses a DC level shifter, implemented through a source-follower stage (M3), which maintains low-voltage operation while enhancing bias stability, as shown in Fig. 2.11.

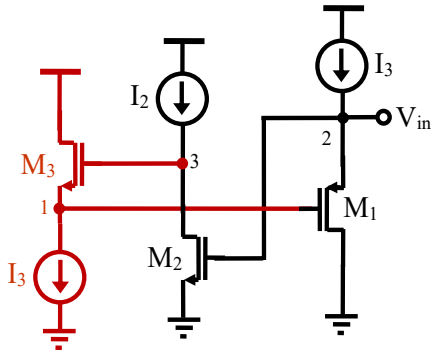


Fig. 2.11 Simplified schematic of low-voltage (low-power) gyrator-C AI proposed by Sae-Ngow & Thanachayanont (2003).

3.5 Synergistic Integration of Performance Enhancement Techniques in Gyrator–C Active Inductors

By combining different enhancement techniques can result in a much larger improvement in the performance of gyrator-C AIs. Various techniques, including such as feedback resistance tuning, cascode stages, extra capacitors, and optimal biasing schemes, are introduced to alleviate specific parasitic effects or constraints.

For example, feedback resistance tuning boosts inductance and quality factor, cascode, or regulated cascode stages suppress parasitic capacitances, and improves high-frequency behavior. A capacitor allows the independent tuning of inductance and series resistance, while an optimized biasing ensures both tunability and low power consumption.

This hybrid approach has to carefully balance various trade-offs, including increased circuit complexity, layout constraints, and possible interaction between the various tuning parameters. On the other hand, several practical implementations reported in literature have demonstrated that the active inductor Q-factors, resulting from hybrid enhancement schemes, can easily exceed 1000, while offering inductance tunability over more than 2–3× range and stable operation up to several gigahertzes. The following

schematics, Fig. 2.12 and Fig. 2.13 will demonstrate example configurations that can successfully combine such techniques.

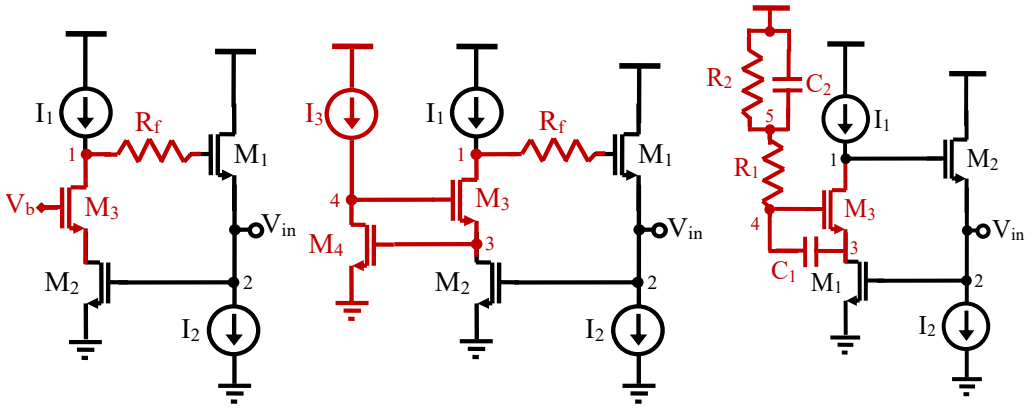


Fig. 2.12 A modified gyrator–C-based AIs that use feedback resistance and cascode transconductors proposed by: (a) Hsiao et al. (2002), Robert et al. (2011), (b) Liang et al. (2005), and (c) Nair et al. (2007).

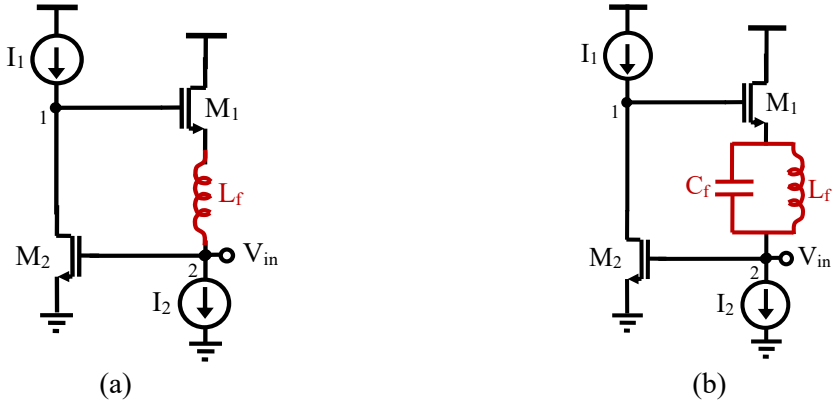


Fig. 2.13 A modified gyrator–C-based AIs that use: (a) feedback spiral inductor, and (b) feedback LC resonance circuit proposed by Seo et al. (2007).

A particular case of active inductor that was proposed by Yodprasit-Ngarmnil, the implementation was based on the dual-feedback transconductor topology, where two complementary feedback mechanisms operate in tandem to achieve high performance (Yodprasit & Ngarmnil, 2000). As illustrated in Fig. 2.14(a) the negative-feedback network is arranged to synthesize an inductive input impedance in such a way that the structure will emulate the desired frequency-dependent behavior. Meanwhile, a positive feedback loop is added which creates a negative resistance.

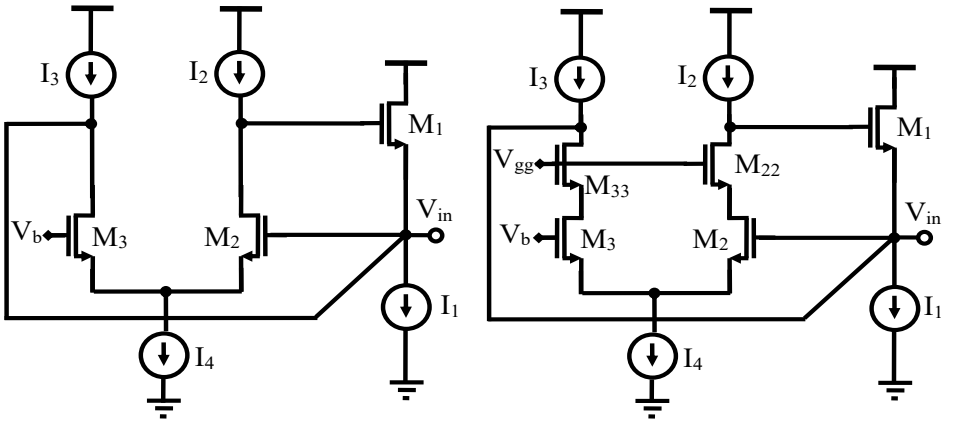


Fig. 2.14 A modified gyrator–C-based AIs that use: (a) double feedback, and (b) cascode double feedback, mechanisms proposed by Yodprasit & Ngarmnil (2000).

This negative resistance effectively cancels the parasitic series losses that normally degrade the performance of the inductor. The combined action of both feedback paths not only preserves the inductive characteristics over a wide frequency range but also leads to a significant enhancement in the quality factor (Q), making the topology suitable for high-frequency and low-loss applications. Fig. 2.14(b) shows an improved version where a cascode stage has been added to each transistor. This enhancement can further reduce the conductance of each transitor.

Conclusion

This chapter presented a comprehensive study on single-ended gyrator-C active inductors based-on advanced performance enhancement techniques. The basic operation of the gyrator was described through impedance modeling, and how parasitic resistances and capacitances may affect the inductance behavior, Q-factor, and the operational frequency range. Although compact and CMOS-compatible, the basic gyrator-C configuration inherently suffers from low quality-factor, limited tunability range, and degraded noise performance that requires further optimization.

The architectural improvements discussed include the use of feedback resistance for inductance control, cascode and regulated cascode topologies for better high-frequency stability, and auxiliary capacitors to reduce loss mechanisms. Biasing schemes, on the other hand, vary from adaptive to low-power techniques, which allow a better trade-off between performance and power efficiency. By combining these methods, the Q-factor of AIs can be increased, leading to higher tuning ranges and better stable performance over wide frequency bands.

References

Abdalla, M. A., Phang, K., & Eleftheriades, G. V. (2006). A 0.13-$\mu $ m CMOS Phase Shifter Using Tunable Positive/Negative Refractive Index Transmission Lines. IEEE microwave and wireless components letters, 16(12), 705-707.

Chen, G. C., Chen, W. Z., & Luo, R. H. (2002, August). A 2.5 Gbps CMOS laser diode driver with preemphasis technique. In Proceedings. IEEE Asia-Pacific Conference on ASIC, (pp. 65-68). IEEE.

DiClemente, D., & Yuan, F. (2007). Current-mode phase-locked loops—A new architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 54(4), 303-307.

Ebrahimi, A., & Shaterian, M. (2024). A 4-bit active-inductor-based digitally programmable low noise amplifier (AI-DPLNA) with a tunable and reconfigurable structure. Microelectronics Journal, 151, 106316.Saad, S., Mhiri, M., Hammadi, A. B., & Besbes, K. (2016). A new low-power, high-Q, wide tunable CMOS active inductor for RF applications. IETE journal of research, 62(2), 265-273.

Ghorbel, I., Haddad, F., Rahajandraibe, W., Barthélemy, H., Loulou, M., & Mnif, H. (2011, December). Design and implementation of an active inductor based LC oscillator. In ICM 2011 Proceeding (pp. 1-4). IEEE.

Hammadi, A. B., Mhiri, M., Haddad, F., Saad, S., & Besbes, K. (2017). An enhanced design of multi-band RF band pass filter based on tunable high-Q active inductor for nano-satellite applications. Journal of Circuits, Systems and Computers, 26(04), 1750055.

Hammadi, A. B., Mhiri, M., Haddad, F., Saad, S., & Besbes, K. (2017). An enhanced design of multi-band RF band pass filter based on tunable high-Q active inductor for nano-satellite applications. Journal of Circuits, Systems and Computers, 26(04), 1750055.

Hsiao, C. C., Kuo, C. W., Ho, C. C., & Chan, Y. J. (2002). Improved quality-factor of 0.18-μm CMOS active inductor by a feedback resistance design. IEEE Microwave and Wireless Components Letters, 12(12), 467-469.

Karsilayan, A. I., & Schaumann, R. (2000, August). A high-frequency high-Q CMOS active inductor with DC bias control. In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (Cat. No. CH37144) (Vol. 1, pp. 486-489). IEEE.

Ler, C. L., A'ain, A. K. B., & Kordesch, A. V. (2009). CMOS active inductor linearity improvement using feed-forward current source technique. IEEE transactions on microwave theory and techniques, 57(8), 1915-1924.

Li, C., Wang, P., & Gong, F. (2011). A low-power active inductor with improved Q-factor and its application to phase shifter. Analog Integrated Circuits and Signal Processing, 66(2), 303-307.

Liang, K. H., Ho, C. C., Kuo, C. W., & Chan, Y. J. (2005). CMOS RF band-pass filter design using the high quality active inductor. IEICE Transactions on Electronics, 88(12), 2372-2376.

Manetakis, K., Park, S. M., Payne, A., Setty, S., Thanachayanont, A., & Toumazou, C. (1996, May). Wideband CMOS analog cells for video and wireless communications. In IEE Colloquium on Wideband Circuits, Modelling and Techniques (pp. 6-1). London UK: IEE.

Momen, H. G., Yazgi, M., Kopru, R., & Saatlo, A. N. (2016). Design of a new low loss fully CMOS tunable floating active inductor. Analog Integrated Circuits and Signal Processing, 89(3), 727-737.

Mukhopadhyay, R., Park, Y., Sen, P., Srirattana, N., Lee, J., Lee, C. H., ... & Laskar, J. (2005). Reconfigurable RFICs in Si-based technologies for a compact intelligent RF front-end. IEEE Transactions on Microwave Theory and Techniques, 53(1), 81-93.

Nair, M. U., Zheng, Y., & Lian, Y. (2007, September). An active inductor based low-power UWB LNA. In 2007 IEEE International Conference on Ultra-Wideband (pp. 813-816). IEEE.

Pakasiri, C., Hsu, K. C., & Wang, S. (2024). A compact 0.73~ 3.1 ghz CMOS VCO based on Active-Inductor and Active-Resistor topology. Journal of Low Power Electronics and Applications, 14(2), 18.

Robert, F., Cathelin, P. H., Die, A., Villegas, M., Epifano, F., Triaire, P., & Baudoin, G. (2011, April). A highly linear and tunable feed forward current source active inductor in 65nm CMOS technology for mobile applications. In WAMICON 2011 Conference Proceedings (pp. 1-6). IEEE.

Saad, S., Ben Hammadi, A., & Haddad, F. (2025). Design and Realization of a High-Q Grounded Tunable Active Inductor for 5G NR (FR1) Transceiver Front-End Applications. Sensors, 25(10), 3070.

Saberkari, A., Ziabakhsh, S., Martinez, H., & Alarcon, E. (2014). Design and comparison of flipped active inductors with high quality factors. Electronics letters, 50(13), 925-927.

Saberkari, A., Ziabakhsh, S., Martinez, H., & Alarcón, E. (2016). Active inductor-based tunable impedance matching network for RF power amplifier application. Integration, 52, 301-308.

Sackinger, E., & Guggenbuhl, W. (2002). A high-swing, high-impedance MOS cascode circuit. IEEE Journal of Solid-state circuits, 25(1), 289-298.

Sae-Ngow, S., & Thanachayanont, A. (2003, October). A low-voltage, wide dynamic range CMOS floating active inductor. In TENCON 2003. Conference on Convergent Technologies for Asia-Pacific Region (Vol. 4, pp. 1460-1463). IEEE.

Seo, S., Ryu, N., Choi, H., & Jeong, Y. (2007, June). Novel high-Q inductor using active inductor structure and feedback parallel resonance circuit. In 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium (pp. 467-470). IEEE.

Szczepkowski, G., Baldwin, G., & Farrell, R. (2007, August). Wideband 0.18 μm CMOS VCO using active inductor with negative resistance. In 2007 18th European Conference on Circuit Theory and Design (pp. 990-993). IEEE.

Thanachayanont, A. (2002, December). CMOS transistor-only active inductor for IF/RF applications. In 2002 IEEE International Conference on Industrial Technology, 2002. IEEE ICIT'02. (Vol. 2, pp. 1209-1212). IEEE.

Thanachayanont, A., & Payne, A. (1996). VHF CMOS integrated active inductor. Electronics letters, 32(11), 999-1000.

Uyanik, H. U., & Tarim, N. (2007). Compact low voltage high-Q CMOS active inductor suitable for RF applications. Analog integrated circuits and signal processing, 51(3), 191-194.

Wang, S., & Wang, R. X. (2012). A tunable CMOS Wilkinson power divider using active inductors. AEU-International Journal of Electronics and Communications, 66(8), 655-658.

Wei, C. C., Chiu, H. C., & Feng, W. S. (2005, November). An ultra-wideband CMOS VCO with 3-5 GHz tuning range. In 2005 IEEE International Wkshp on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Comm & Wireless Sensor Networks (pp. 87-90). IEEE.

Weng, R. M., & Kuo, R. C. (2007, July). An ω 0-Q tunable CMOS active inductor for RF bandpass filters. In 2007 International Symposium on Signals, Systems and Electronics (pp. 571-574). IEEE.

Wu, M. J., Huang, Y. Y., Lee, Y. H., Mu, Y. M., & Yang, J. T. (2007). Designs of CMOS multi-band voltage controlled oscillator using active inductors. Int. J. Circuits, Syst. Signal Process, 1(2), 207-210.

Xiao, H., & Schaumann, R. (2002, May). Very-high-frequency lowpass filter based on a CMOS active inductor. In 2002 IEEE International Symposium on Circuits and Systems (ISCAS) (Vol. 2, pp. II-II). IEEE.

Xiao, H., & Schaumann, R. (2002, September). A low-voltage low-power CMOS 5-GHz oscillator based on active inductors. In 9th International Conference on Electronics, Circuits and Systems (Vol. 1, pp. 231-234). IEEE.

Xiao, H., & Schaumann, R. (2007). A 5.4-GHz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology. Analog integrated circuits and signal processing, 51(1), 1-9.

Xiao, H., Schaumann, R., Daasch, W. R., Wong, P. K., & Pejcinovic, B. (2004, May). A radio-frequency CMOS active inductor and its application in designing high-Q filters. In 2004 IEEE International Symposium on Circuits and Systems (ISCAS) (Vol. 4, pp. IV-197). IEEE.

Yodprasit, U., & Ngarmnil, J. (2000, May). Q-enhancing technique for RF CMOS active inductor. In 2000 IEEE International Symposium on Circuits and Systems (ISCAS) (Vol. 5, pp. 589-592). IEEE.

Yuan, F. (2008). CMOS active inductors and transformers: principle, implementation, and applications. Boston, MA: Springer US.