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Chapter 1: Foundations and Techniques of Active Inductors Design in CMOS RF Circuits

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Abstract: Recently, active inductors have emerged as an appealing alternative to conventional on-chip spiral passive inductors within radio-frequency (RF) integrated circuits. Unlike passive inductors, which occupy large silicon area and are fixed, active inductors emulate the real inductive behavior using active devices such as MOSFETs and capacitors, thereby realizing compact size, electronic control, and compatibility with standard CMOS processes. The theory of active inductors is reviewed in this chapter, starting from the very basics of inductance and comparing the passive versus the active implementations. Amplifier-based, current conveyor-based, and gyrator-C topologies of active inductors are reviewed along with their relative merits and trade-offs. Emphasis has been placed on the gyrator-C structure since it is one of the two broad classes of topologies highly commendable for tunability and ease of integration. Then, design considerations for both the single-ended and differential topologies followed by presenting various techniques to improve performance figures of merit, which include quality factor (Q), inductance tuning, noise, linearity, stability, and power consumption, are presented. Combining theoretical insight with practical design strategies, this chapter provides the foundation for applying active inductors in RF and microwave systems, especially in filters, oscillators, and impedance-matching networks.

Keywords: Active Inductor, Gyrator-C, CMOS, Tunability, Optimization Methods, Single-Ended, Differential.

1 Introduction

Inductors are among the fundamental components in the design of analog and RF circuits. They find a wide range of applications in filters, oscillators, impedance matching networks, and tuned amplifiers. For integrated circuits, especially for RF front-end use, inductors are a critical factor that greatly decides the performance of resonant

circuits and frequency-selective networks. Implementation of inductors on silicon, however, faces serious challenges. The implementation of classical spiral inductors requires large silicon area, is not easily tuneable after fabrication, and usually exhibits poor Q-factors, particularly at low frequencies. Such disadvantages have presently stirred intensive efforts toward alternative solutions compatible with modern CMOS technology to mimic inductor behavior.

One promising alternative is the active inductor, which synthesizes inductive behavior using active circuit elements such as transistors, capacitors, and bias currents. The active inductor differs from passive spiral inductors by providing compact size, electronic tunability, and easier integration with a standard CMOS process, making it hence very appealing for usage in RF integrated circuits, RFICs, where area efficiency and performance flexibility are of necessity.

Active inductors based on the gyrator-C architecture have been first proposed for both GaAs and bipolar technologies Kaunisto et al. (1995) and later adopted for CMOS technology Thanachayanont & Payne (2000); Wu et al. (2001); Grozing et al. (2001). In more recent years, gyrator-C active inductors have been used in place of passive inductors in front-end amplifiers Pletcher et al. (2007); Huang et al. (2004), as well as in tunable impedance matching networks for Internet-of-Things -IoT-applications Saberkari et al. (2016). Other notable applications include high-Q tunable negative inductors for small antennas and analog sensor readout circuits De Dorigo et al. (2015) and use in broadband metamaterials Avignon Meseldzija et al. (2015). In addition, active inductors have found great potential in a large number of other RF applications including voltage-controlled oscillators Cheng et al. (2014), frequency dividers Jang et al. (2009), phase shifters Abdalla et al. (2007), low-noise amplifiers Kia et al. (2013), current-mode phase-locked loops DiClemente et al. (2008), high-order low-pass filters Kumar et al. (2001), high-speed CML latches Payandehnia et al. (2011) and transceivers for high-speed data links Michael Lee et al. (2008).

Despite these benefits, the design issues for active inductors include noise and linearity and stability problems which must be addressed with much care. The rest of the chapter is organized as follows:

This chapter is organized as follows: Section 2 introduces the basics of inductance by first defining inductors and their fundamental principle of energy storage, together with the important voltage–current relationships. A comparison between the spiral passive inductor and the active inductor is also treated. Section 3 presents the general theory behind the active inductor. The concept of the synthetic inductor is introduced, along with the main active architectures used in practice. A comparison of the main amplifier-based, current conveyor-based, and gyrator-C topologies outlines their advantages and shortcomings. Section 4 is dedicated to gyrator-C active inductors, both single-ended

and differential. Derivation of their equivalent circuit model is provided along with an explanation of their operation principle, with particular emphasis on loss mechanisms and parasitic effects. Section 5 covers advanced design techniques for improving active inductor performance, namely self-resonant frequency optimization, Q-factor enhancement, tuning methods, noise reduction techniques, linearity enhancement, stability control, and power consumption reduction. Section 6 concludes this chapter by summarizing the main contributions. The role of active inductors toward enabling compact and reconfigurable RF circuits is emphasized.

2 Basic of Inductance

2.1 What's an Inductor?

An inductor is a passive electrical component that can store energy in a magnetic field created by the electrical current flowing through it. The fundamental property of an inductor is called the inductance denoted by L and measures in Henry (H). Inductance quantifies the ability of the inductor to oppose changes in current, a behaviour governed by Lenz's law. As shown from the signal flow diagram represented in Fig. 1.1, the basic voltage-current relationship for an ideal inductor is described by:

$$V(t) = L\frac{d(t)}{dt} \Rightarrow V(s) = sL.I(s) \quad (1)$$

where V(t) is the voltage across the inductor, I(t) is the current through the inductor, 's' is the Laplace variable (s=jω) and 'L' is the inductance in Henry.

This equation shows that the voltage across an inductor is proportional to the time derivative of the current: When a current is increasing or decreasing, the inductor produces a back electromotive force (EMF) that is opposite to the change in current.

Inductors store energy in their magnetic fields. The energy E, stored in an inductor at any instant of time is given by the following equation:

$$E = \frac{1}{2}LI^2 \quad (2)$$

This property makes inductors indispensable in circuits designed for energy transfer or storage, like resonators, filters, and power management systems.

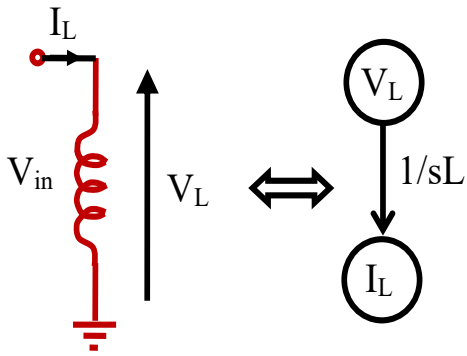

Fig. 1.1 Ideal inductor and its signal flow graph representation.

2.2 Spiral Inductors versus Active Inductors: A Brief Comparison

Spiral inductors represent the most frequently used on-chip inductive elements for conventionally designed RF and analog circuits. These are usually fabricated using a planar spiral geometry by patterning metal traces on a silicon substrate, accessed by both CMOS and BiCMOS processes. The current flowing through a spiral forms a loop path and creates a magnetic field, similar to a conventional wire-wound inductor. Spiral inductors are widely used in a number of RF circuits, such as filters, oscillators, and impedance matching networks.

One of the major advantages with spiral inductors is that they can operate passively. Because they do not use bias currents, they do not consume any DC power and are thus intrinsically very power-efficient. The design is also fairly simple, based on mature fabrication techniques, routine in RF circuit design. When adequately optimized for high-frequency operation, the spiral inductor can have a high quality factor, especially at gigahertz frequencies, and hence finds application in resonant circuits at such frequencies.

Spiral inductors, however, also raise important limitations, particularly in the case of their integration into modern, high-density IC designs. The main drawback is the large silicon area they take up, which significantly increases fabrication costs and limits miniaturization. Spiral inductors are unfortunately afflicted by a low Q-factor at lower frequencies, due to substrate losses and parasitic capacitances. Another drawback is that the value of spiral inductors is fixed by fabrication and cannot be tuned; one has to physically rework the circuit for changes. Their performance is highly process-dependent, too, as variations in metal thickness, substrate properties, and layout design all affect inductance and Q-factor.

In overcoming these challenges, designers often turn to active inductors, whose physical coil is replaced by active electronic components, typically MOSFET transistors, capacitors, and biasing circuits. The most common implementation of an active inductor is based on the concept known as gyrator-C, in which two transconductance stages emulate inductive behavior by converting voltage to current and vice-versa, with a capacitor providing energy storage.

Active inductors possess a number of advantages compared to spiral inductors. First, they provide a compact size with much less silicon area, critical for high-density IC integration. Second, active inductors offer electronic tunability, that is, both the inductance value and the quality factor can be adjusted dynamically by varying bias currents or control voltages. This tunability is particularly appealing for adaptive RF circuits and post-fabrication calibration. Active inductors also represent full compatibility with standard CMOS processes, easing integration into mixed-signal and RF systems without any special fabrication steps. They can also be designed for operation over an extended frequency range, well beyond those for which passive spiral inductors become impractical due to strong parasitic effects.

Despite these merits, active inductors bring about some problems. They will continuously dissipate power due to their biasing currents required by the transistors and therefore are undesirable in power-conscious circuits. They add more noise as well, which is undesirable in low-noise RF circuits. Nonlinearity is another issue; for instance, a MOSFET-based transconductance circuit can easily show distortion in case of large signal amplitudes. Last but not least, active inductors may be prone to instability; unwanted oscillations may easily occur because there could be some feedback loops along with parasitic elements. This has to be avoided by careful design. Table 1.1 compares some basic characteristics of spiral inductors with active ones.

Table 1.1 Key differences between spiral and active inductors.

Feature	Spiral inductor	Active inductor
Implementation	Metal spiral on silicon	Transistors + capacitors
Silicon area	Large	Small (compact design)
Power consumption	None (passive component)	Requires bias current (active)
Tunability	Fixed (post-fabrication)	Electrically tunable
Quality factor (Q)	Moderate at GHz, low at low freq	Medium to high, but tunable
Integration in CMOS	Limited by size and process	Fully CMOS-compatible
Frequency range	Limited by parasitics	Adjustable via design parameters
Noise performance	Low (passive)	Higher (due to active devices)
Linearity	High	Moderate, design-dependent
Stability	Stable	Potential oscillation risk

3 Theory of Active Inductors

3.1 Concept of Synthetic Inductance

An active inductor is a circuit that emulates the behavior of a passive inductor by using active components like transistors, capacitors, and current sources. Unlike physical inductors that store energy in a magnetic field, active inductors synthesize an equivalent inductive impedance through active circuitry by controlling the voltage-current relationship.

A number of architectures have been proposed to implement active inductors; each based on different analog circuit principles. Each has its unique operational principles and benefits and limitations. The most widely recognized implementations are the following:

- *Amplifier-based active inductors*

Basically, an active inductor synthesizes inductive behavior by means of an amplifier and associated feedback. Because of the controlled feedback in the amplifier circuit, its input impedance is changed so as to present a positive reactance that mimics an inductor within a certain frequency range.

- *Current Conveyor-based active inductors*

Current Conveyors (CCII) are multifunctional analog building blocks of circuits that can implement inductive behavior. A current conveyor is able to provide a high-speed current transfer between its terminals with specific voltage-current relationships which can then be manipulated to emulate inductance.

- *Gyrator-C based active inductors*

The most widespread and widely-researched (especially in CMOS-technology) form of realization of active inductors is the gyrator-C topology. It takes two transconductance stages (gyrators) and a capacitor to transform capacitive reactance at the input port to inductive reactance.

3.2 Active Inductor Topologies Comparison

The comparison among the different types of active inductors reflects various trade-offs among these design approaches. Each has different advantages and disadvantages, which are strongly dependent on the target application. As seen from Table 1.2, amplifier-based active inductors offer simplicity and flexibility in design, making them applicable for low-frequency applications where circuit complexity should be minimized. Unfortunately, they show limited high-frequency performance due to intrinsic gain-

bandwidth limitations of amplifiers and often introduce additional noise and higher power dissipation. Current conveyor-based active inductors provide better high-frequency operation with low input impedance, which is advantageous in some RF applications. Their simple implementation is appealing, but they can easily become nonlinear for large signal conditions and, often, lack an explicit method for dynamic tunability. In contrast, gyrator-C based active inductors have become the most widely used in modern integrated circuit design; indeed, they can be compact, fully compatible with CMOS processes, and provide electronic tunability of both inductance and quality factor. These advantages come at the cost of power consumption due to continuous bias currents in gyrator-C implementations, additional noise due to active devices, and careful design to avoid instability due to feedback and parasitic effects. Choosing the proper active inductor architecture depends on balancing these characteristics to meet performance, area, power, and integration requirements of the intended application.

Table. 1.2 Summary of active inductor architectures: benefits and limitations.

Type	Advantages	Disadvantages
Amplifier based AI	Simple design, flexible, suitable for low-frequency	Limited bandwidth, higher power, more noise
Current Conveyor based AI	High-speed, simple circuit, low input impedance	Nonlinear behavior, limited tunability
Gyrator-C based AI	Compact, tunable, widely used, CMOS-compatible,	Power consumption, noise, stability issues

4 Principles of Lossy Gyrator-C Active Inductor

Active inductors can be implemented with various circuit configurations depending on application, performance requirements, and integration constraints. Two major categories dominate the literature and practice: single-ended and differential topologies. Each has its unique advantages and trade-offs for noise, linearity, power consumption, and area.

4.1 Single-Ended Active Inductor

The single-ended active inductor is the simplest and most researched topology. The configuration, shown in Fig. 1.2, incorporates a capacitive shunt feedback network that acts as an impedance inverter, which essentially converts capacitive reactance to inductive reactance at the input port.

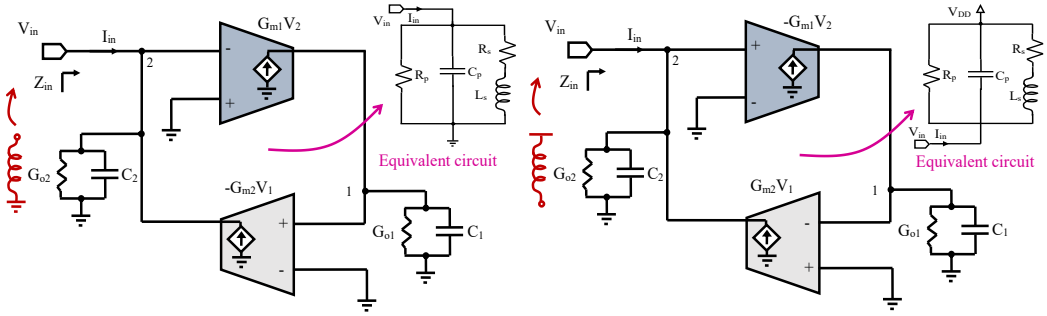

Fig. 1.2 Gyrator-C circuit block diagram terminal connected to: (a) ground, (b) power supply, with their equivalent RLC models.

G_{m1} is the first-stage transconductance amplifier, configured in an inverting mode. This converts the applied input voltage into a current driving the capacitor to produce a voltage that is 90° lagged with respect to the input voltage. In turn, this is applied to the transconductance amplifier G_{m2}, whose non-inverting output then provides an output current. Overall, the successive conversions of voltage to current, integration by the capacitor and conversion back to current give a net impedance proportional to frequency, emulating an ideal inductor. Although effective, this implementation imposes limitations in voltage swing given the nature of operation of the MOSFETs in the stages of transconductance. The minimum and maximum input voltages should be above $V_{T+}V_{ov}$ and below $V_{DD}-V_T-V_{sat}-V_{ov}$, respectively, with V_T for the threshold voltage of MOSFETs, V_{ov} for the overdrive voltage, V_{DD} for the supply voltage, and V_{sat} accounting for the voltage drop across the bias current source I_1. These directly affect the dynamic range and linearity of the active inductor, especially in large-signal operations.

The gyrator-C network is more complete in that, when non-idealities are included, it models losses and parasitic effects. In Fig. 1.2, the total shunt conductance and capacitance at the input port are denoted by g_{o1} and C_1 while at the output port g_{o2} and C_2 represent those quantities, respectively. The system behavior is described by the transconductance relations:

$$G_{m1}V_2 = (G_{o1} + sC_1)V_1 \tag{3}$$

$$I_{in} = G_{m2}V_1 + (G_{o2} + sC_2)V_2 \tag{4}$$

where G_{o1} and G_{o2} are the total conductances at the input and output ports, and V_1 and V_2 are the corresponding voltages. By using the above relationships, the following expression for the admittance looking into port 2 of the gyrator–C network can be derived:

$$Y_{in} = \frac{1}{Z_{in}} = s\frac{1}{G_p} + \frac{1}{R_p} + \frac{1}{sL_s + R_s} = G_{o2} + sC_2 + \frac{G_{m1}G_{m2}}{sC_1 + G_{o1}} \quad (5)$$

This expression shows that the input impedance behaves as a lossy inductor in parallel with parasitic elements, including resistances and capacitances due to the MOSFET devices and the circuit layout. The resulting equivalent circuit can be represented by an inductor L_s in series with a resistor R_s, all shunted by a parallel resistor R_p and a parallel capacitor C_p. The following relationships governing these elements have been derived as:

$$L_s = \frac{C_1}{G_{m1}G_{m2}} \quad (6)$$

$$R_s = \frac{G_{o1}}{G_{m1}G_{m2}} \quad (7)$$

$$R_p = \frac{1}{G_{o1}} \quad (8)$$

$$C_p = C_2 \quad (9)$$

Here L_s is the synthesized inductance, R_s represents series loss resistance, R_p models the parallel loss path given finite output conductance of the second transconductance stage and C_p accounts for the parasitic capacitance at port 2 dominated by the MOSFET gate capacitances and interconnect parasitics.

Single-ended topology: advantages and disadvantages

(+) Compact: It occupies minimal silicon area and therefore is suitable for high-density integration.
(+) Easy to implement: The design uses basic transistor structures and is straightforward.
(+) Electronic tunability: Inductance and quality factor can be tuned by changing bias currents or capacitor values.
(+) Low power: With a relative simplicity of biasing schemes, there is often reduced overall power consumption compared to more complicated topologies.

(-) Noise susceptibility: No common-mode noise rejection; susceptible to substrate and power supply noise.
(-) Limited linearity: Nonlinear behavior may be expected for high signal amplitudes because of changing MOSFET transconductance.
(-) Asymmetrical operation: Only suitable for circuits that do not require differential signaling.
(-) Potential stability issues: The feedback path should be carefully designed so that no unwanted oscillations take place.

4.2 Principles of Lossy Gyrator-C Active Inductor

A second critical option in designing active inductors is the floating active inductor, in which both terminals of the synthetic inductor are not connected to the ground or to the power supply. This structure, also commonly referred to as a differential or floating active inductor, is shown in Fig. 1.3. Floating active inductors are crucial in both RF and analog systems where symmetric fully differential signal paths are required for enhancing noise immunity, increasing linearity, and directly interfacing with differential circuits.

The floating gyrator–C active inductor can be obtained by extending the single-ended gyrator–C topology in a differential configuration. This is realized by replacing the single-ended transconductors with differentially configured OTAs. The circuit, shown in Fig. 1.3 with the interrupted line, includes both the input and output conductance and capacitance contributions of the OTAs and represents a more accurate and realistic model.

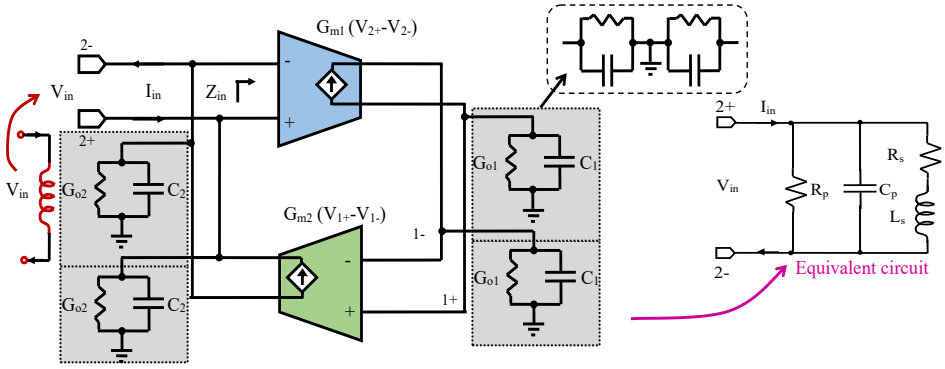

Fig. 1.3 Floating gyrator-C based AI block diagram, with it equivalent RLC model.

For the differential active inductor, the admittance looking into port 2 of the gyrator–C network is given by:

$$Y_{in} = \frac{1}{Z_{in}} = s\frac{1}{G_p} + \frac{1}{R_p} + \frac{1}{sL_s + R_s} = \frac{G_{o2}}{2} + \frac{sC_2}{2} + 2\frac{G_{m1}G_{m2}}{sC_1 + G_{o1}} \qquad (10)$$

The equivalent circuit of the differential active inductor shown in Fig. 1.3 can be defined by the following component values:

$$L_s = \frac{C_1/2}{G_{m1}G_{m2}} \qquad (11)$$

$$R_s = \frac{G_{o1}/2}{G_{m1}G_{m2}} \qquad (12)$$

$$R_p = \frac{2}{G_{o1}} \tag{13}$$

$$C_p = \frac{C_2}{2} \tag{14}$$

These equations are similar to the single-ended situation, but now parasitic effects at both the input and output of each OTA are included, so the differential model is more complete and representative of realistic circuit behaviour.

Some of the major advantages of differential active inductors over their single-ended counterparts make them very suitable for state-of-the-art RF and mixed-signal integrated circuits:

- *Higher voltage swing:* The voltage swing in a differential active inductor can be almost twice as large for a comparable single-ended inductor. The rationale is that, since the signal is expressed as a difference between two nodes, this effectively doubles the permissible input range while maintaining transistor operation in the desired region. Increased dynamic range, this is a very important advantage of differential active inductors and a strong reason for their use in high-performance RF applications.
- • *Common-mode noise rejection and harmonic suppression:* As in any differential circuit, the differential active inductor inherently rejects common-mode interference such as power supply noise and substrate coupling. This is especially welcome in SoC designs where highly noisy digital circuits share the same substrate with sensitive analog circuits. Furthermore, even-order harmonics are suppressed in a differential arrangement, ensuring better linearity. This is of paramount importance to avoid the corruption of signals in communication systems where intermodulation distortion has to be kept at a minimum.
- • *Suitability for oscillator design:* Most RF oscillators, and in particular LC voltage-controlled oscillators (VCOs), require 50% duty cycle for symmetric oscillation waveforms and for mitigation of phase noise. Differential active inductors, which naturally provide balanced and differential outputs, are easily interfaced with a fully differential oscillator core, making them favorites in modern RF design for PLLs and frequency synthesizers.

Besides these, active differential inductors have better immunity to substrate coupling and are less sensitive to layout-induced mismatches, hence being more robust for practical IC implementations. In general, though, this benefit comes with increased circuit complexity, higher power consumption, and a larger silicon area compared to single-ended designs. The designer has to intelligently balance these based on the demands of the specific application.

5 Techniques to Enhance Active Inductor Performance

5.1 Self-Resonant Frequency and Frequency Response

The self-resonance frequency of the active inductor is dominated by the interaction between the equivalent inductance L_s and the parallel parasitic capacitance C_p, giving:

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \tag{15}$$

This expression can be rewritten in terms of the transconductance cut-off frequencies of the two OTAs: $\omega_{t1}=g_{m1}/C_1$ and $\omega_{t2}=g_{m2}/C_2$. Thus, the self-resonant frequency becomes:

$$\omega_0 = \sqrt{\omega_{t1}\omega_{t2}} \tag{16}$$

Typically, this indicates that the maximum operating frequency of a lossy active inductor is directly proportional to the transconductance product of the OTAs and inversely proportional to the parasitic capacitances at both ports. The circuit behaves inductively up to this resonance frequency, beyond which the capacitive parasitics become dominant.

In practical implementations, the behavior of the active inductor is frequency-dependent and defined by a pole-zero structure. The input impedance of the RLC equivalent circuit of the lossy active inductor is given by:

$$Z_{in} = \frac{R_s}{C_pL_s} \cdot \frac{s\frac{L_s}{R_s}+1}{s^2 + s\left(\frac{L_s + R_sR_pC_p}{R_pC_pL_s}\right) + \frac{R_s+R_p}{R_pC_pL_s}} \tag{17}$$

By examining this expression, Z_{in} has the zero frequency occuring at:

$$\omega_z = \frac{R_s}{L_s} \tag{18}$$

This is the frequency where the inductive reactance starts to dominate over the series resistance. When the system exhibits a pair of complex conjugate poles, the resulting resonant frequency is dictated by the interaction of the parasitic elements, and is calculated as follows:

$$\omega_p = \sqrt{\frac{R_p+R_s}{R_pC_pL_s}} \tag{19}$$

Since R_s is always smaller than R_p, for simplification R_s is ignored and ω_p is approximated as follows:

$$\omega_p \approx \sqrt{\frac{1}{C_p L_s}} \approx \frac{1}{C_p R_p} = \omega_0 \tag{20}$$

At frequencies beyond ω_p, the inductive behavior is compromised as the circuit transitions into a capacitive region due to the dominance of parasitic capacitance.

Beyond ω_p, the inductive behavior is degraded since the circuit enters into a capacitive region because the effect of parasitic capacitance is dominating. Overall, ω_z and ω_p mark the frequency range inside which the gyrator–C-based active inductor emulates the real inductor. It was already derived from the Bode plot of Z_{in} in Fig. 1.4 that the circuit behaves as an inductor within this frequency range. Of course, it is dominated by the resistive losses below ω_z and is dominated by the capacitive effects beyond ω_p. Fundamentally, the upper bound of the usable frequency range is determined by the self-resonant frequency ω_0, which itself is limited by the cut-off frequencies of the transconductors in the active inductor. Hence the bandwidth of inductive behavior is limited both by the active device characteristics and the parasitic elements associated with the circuit.

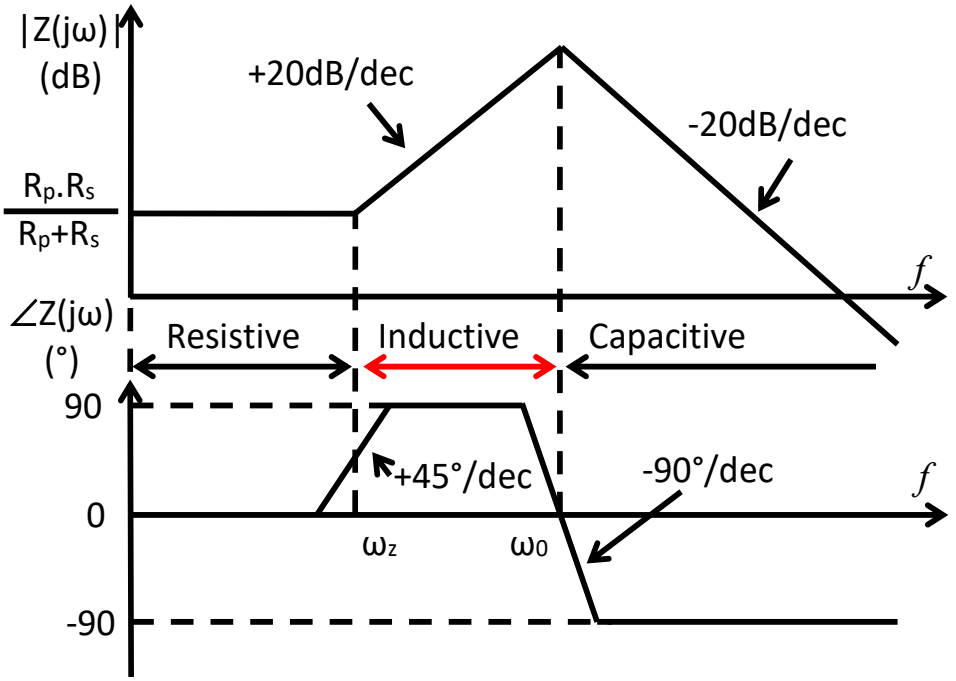

Fig. 1.4 Magnitude and phase plots of the input impedance of a lossy gyrator-C based AI.

5.2 Quality Factor (Q) Enhancement

One of the most important parameters for judging the performance of an active inductor is its quality factor, defined as the ratio of stored energy to the energy dissipated per cycle. For a linear inductor including active inductor, Q can be expressed as:

$$Q = \frac{\Im m(Z)}{\Re e(Z)} \tag{21}$$

Ideally, Q is defined by the inductive reactance over the series resistance. However, for a practical gyrator–C-based active inductor, the most important parasitic elements, such as the series resistance R_s, parallel resistance R_p, and parallel capacitance C_p, cannot be neglected since they contribute to the frequency response of the whole circuit as well as to the loss characteristic. Accounting for the effects caused by them, the detailed expression of the Q-factor of a lossy active inductor is given by:

The more complete expression for the Q-factor of a lossy active inductor including these parasitic elements is given by:

$$Q = \frac{\omega L_s}{R_s} \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L_s}{R_s}\right)^2\right]} \left[1 - \frac{R_s^2 C_p}{L_s} - \omega^2 L_s C_p\right] \tag{22}$$

This equation includes the interaction between the ideal inductive component and non-ideal parasitics. In the numerator, the terms describe the resonance behavior, whereby $\omega^2 L_s C_p$ represents the capacitive parasitic effect and $(R_s^2 C_p)/L_s$ represents loss contributions from $R_s C_p$ interaction. The denominator reveals how R_s and R_p both degrade Q by introducing resistive loss paths.

$$Q \approx \frac{\omega L_s}{R_s} \tag{23}$$

The $\omega^2 L_s C^p$ term is negligible at low frequencies, and the expression reduces approximately to the simpler form:

One common technique to enhance the Q-factor introduces negative resistance compensation, usually through Q-enhancement circuits. This method adds a controlled amount of negative resistance in series with the active inductor, and with proper design, it can cancel a part of R_s, thus acting to decrease the denominator of the Q expression. If such a negative resistance R_{neg} is introduced:

$$R_{eff} = R_s + R_{neg} \tag{24}$$

Substituting R_{eff} into the detailed Q equation, the updated quality factor is:

$$Q = \frac{\omega L_s}{R_{eff}} \frac{1 - \left(\frac{R_{eff}^2 C_p}{L_s} - \omega^2 L_s C_p \right)}{1 + R_{eff} \left(1 + \left(\frac{\omega L_s}{R_{eff}} \right)^2 \right) \Big/ R_p} \tag{25}$$

This equation shows that Q-enhancement directly impacts the inductor's performance, since by properly choosing the value of R_{neg}, R_{eff} is reduced and the magnitude of Q increases. In the ideal limit, if $R_{eff} \rightarrow 0$, the Q-factor goes to infinity; however, this cannot be realized practically. Trying to completely cancel R_s will most likely be unstable because negative resistance may accidentally create an oscillation condition if R_{eff} becomes negative. The goal of the design is to partially cancel R_s, thus maximizing Q while keeping the circuit stable and the phase margin adequate.

Besides, inductive behavior bandwidth reduces with increasing Q, showing the traditional trade-off between selectivity and bandwidth. High Q is thus preferred for narrowband RF filters and resonators, while moderate Q values may be selected for broadband matching networks to keep bandwidth. Possible enhancement methods are:

- *Negative resistance compensation*: This negative resistance compensates for part of the parasitic series resistance Rs and increases the effective Q by lowering the denominator of the Q expression. Usually, this is accomplished by properly biasing a MOSFET, either in a cross-coupled pair configuration or with appropriate feedback-biasing, to create a negative small-signal resistance at the point of interest. This technique can be powerful in improving Q but must be designed carefully to avoid excessive negative resistance, which can lead to unwanted oscillations or instability.

- *Transistor sizing optimization*: The dimensions of the MOSFETs in active inductor design affect both transconductance (g_m) and output resistance (r_o). Through careful W/L selection, designers can balance gm to provide sufficient inductance generation while maximizing r_o to minimize parasitic conductance. This is critical because increasing gm generally lowers r_o, so optimal sizing is essential to achieving High-Q without degrading linearity or increasing noise.

- *Current reuse structures*: Current reuse structures allow several transconductance stages to share the same bias current, thereby reducing overall power while maintaining or improving performance. This results not only in improved effective Q by lowering the resistive loading but also helps with integration in low-power RF systems.

- *Feedback techniques:* Positive feedback can be used in a controlled manner to increase the apparent inductance and Q-factor by reinforcing the inductive behavior

of the circuit. However, because positive feedback inherently threatens stability, designers must carefully manage loop gain and provide adequate phase margin to prevent oscillation.

5.3 Tunable Inductance Range

Tunability is a key advantage of active inductors, allowing post-fabrication adjustment of inductance values to accommodate process variations or changing system requirements. Main techniques include:

- *Bias current control*: The most common method, where changing the bias current directly alters gm (since the equivalent inductance of a gyrator–C structure is inversely proportional to $g_{m1}g_{m2}$). Increasing bias current increases g_m, reducing inductance, and vice versa. This provides continuous tuning but can affect linearity and power consumption.
- *Varactor integration*: Replacing the fixed capacitor in the gyrator–C structure with a voltage-controlled varactor enables inductance tuning via voltage control. This method also allows simultaneous tuning of frequency response and Q, but may introduce nonlinearity due to voltage-dependent capacitance.
- *Digital control*: Using digitally controlled current mirrors or DACs to program bias currents or varactor voltages allows precise and repeatable tuning, enabling calibration and real-time adaptive reconfiguration in RF systems.
- *Process variation compensation*: Tunability allows compensation for manufacturing variations by adjusting bias currents or control voltages post-fabrication, ensuring consistent inductance and performance across production lots.

5.4. Noise Reduction

Active inductors produce more noise than passive ones due to active devices like MOSFETs. Key noise sources are thermal noise, flicker noise (1/f), and bias circuit fluctuations. Common noise reduction strategies:

- *Differential topology*: Cancels common-mode noise from substrate, supply, and nearby digital circuits. Differential operation also suppresses even-order harmonics.
- *Low-noise biasing*: Cascode current sources, noise-filtered mirrors, and decoupled bias networks can minimize thermal and flicker noise contributions.

- *Optimized device sizing*: Larger W/L ratios reduce thermal noise by lowering channel resistance but can limit high-frequency performance due to larger gate capacitance; thus, a balance is required.
- *Filtering*: Adding RC filters or decoupling capacitors at bias nodes prevents noise coupling into the active inductor path, especially in mixed-signal ICs.

5.5 Linearity Improvement

Linearity is crucial for RF circuits (mixers, LNAs, VCOs) where distortion degrades performance. Techniques include:

- *Device biasing*: Optimize transistor biasing in the most linear gm region (moderate inversion or saturation) to minimize distortion.
- *Source degeneration*: Adding resistors at transistor sources introduces negative feedback, stabilizing current–voltage behavior and improving linearity at the cost of slightly reduced transconductance.
- *Differential operation*: Cancels second-order distortion due to circuit symmetry.
- *Feedback linearization*: Controlled local feedback around transconductance stages stabilizes g_m across varying input levels, improving linearity without severely affecting Q or stability.

5.6 Enhancement of Stability Methods.

Active inductors are prone to oscillations due to internal feedback. Stability must be ensured using:

- *Pole-zero management*: Avoid excessive impedance peaking by damping complex poles from inductance–capacitance interactions. Ensure resonance lies outside the intended frequency range.

$$\text{pole}_{1,2} = \frac{C_1 + C_2}{2C_1C_2}\left[-1 \pm \sqrt{1 - \frac{4C_1C_2G_{m1}G_{m2}}{\left(C_1 + C_2\right)^2}}\right] \tag{26}$$

$$\xi = \frac{1}{2\sqrt{G_{m1}G_{m2}}}\left[\sqrt{\frac{C_1}{C_2}} + \sqrt{\frac{C_2}{C_1}}\right] \tag{27}$$

- *Phase response analysis:* Check small-signal loop gain and phase margin (~90° typical) across all process, voltage, and temperature (PVT) corners.

- *Controlled Q-enhancement*: Limit negative resistance injection to only partially cancel R_s, maintaining positive R_{eff} for stability.
- *Parasitic control*: Minimize layout-related parasitics using symmetric routing, shielding, guard rings, and isolation to prevent unintentional coupling and frequency shifts.

5.7 Specifically to Powers Consumption Optimization

Although active inductors consume power, this disadvantage can be reduced with careful design.

- *Current reuse techniques*: Designing the circuit so that several transconductance stages share the same bias current can drastically reduce total power consumption without any performance degradation.
- *Bias current optimization*: Choosing the smallest bias current that can meet performance requirements helps balance inductance tuning, bandwidth, and energy efficiency without introducing unnecessary power overhead.
- *Adaptive biasing*: Dynamically adjusting the bias current according to real-time system demands enables low-power operation during idle periods and high performance when needed.
- *Device technology and scaling:* Exploiting advanced CMOS technologies allows for higher transconductance efficiency, enabling lower power operation. However, short-channel effects and leakage currents must be carefully managed.
- *Layout optimization*: Minimizing parasitic elements through careful layout reduces resistive and capacitive losses, allowing the active inductor to function efficiently with lower bias currents.

Conclusion

This chapter has treated all aspects of active inductors, from fundamental principles to advanced design considerations. It started by introducing the concept of inductance and compared passive spiral inductors against active alternatives, underlining the advantages of active implementations, including compact integration, tunability, and CMOS compatibility. Different topologies of active inductors were reviewed with a particular focus on the gyrator-C topology, still the most widely adopted due to its versatility and strong performance. Both single-ended and differential topologies have been analyzed in order to understand how topology affects noise rejection, linearity, and voltage swing.

The chapter further discussed various approaches to enhance active inductor performance, facing issues such as limited Q-factor, parasitic effects, noise, nonlinearity, stability, and power consumption. It covered a number of effective techniques that improve robustness and efficiency: negative resistance compensation, tuning by varactors, differential operation, and adaptive biasing.

In summary, active inductors are a viable option to their passive counterpart, and an effective trade-off between integration density and design freedom may be achieved. Though some issues, mainly noise, linearity, and stability remain unavoidable, the design techniques discussed provide efficient methods for their reduction. These will be the basic principles for the subsequent chapters dealing with active inductor applications in the realm of reconfigurable filters and other RF front-ends.

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