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Chapter 5: Artificial intelligence in electronic design automation: revolutionizing chip design workflows

5.1. Introduction

Electronic design automation (EDA) has been unpredictable. Moore's Law and its extension are no longer valid. Chip design has never been more complex and disruptive, with hundreds of thousands of design engineers working simultaneously around the world on a single chip. Chip design is no longer just a role for seasoned engineers; design methodologies are changing, rules are changing faster, and designers need to adapt rapidly. All of these changes present designers with daunting challenges. This rising complexity, aided by new semiconductor technologies, is propelling researchers towards new horizons.

AI has provided significant solutions to many problems in varied fields, such as speech processing, picture processing, and self-driving cars. There are many subfields of AI, such as Natural Language Processing (NLP) and Machine Learning (ML). In comparison, ML is a subfield of AI, including supervised learning, semi-supervised learning, and unsupervised learning. Deep Learning (DL) is a subfield of ML that includes CNN and RNN. The goals of AI/ML are Learning, Reasoning, Predicting, and Perception. The apparent advantage of AI/ML is its ability to quickly identify the trends and patterns in large volumes of data that may be difficult to find either manually or via traditional algorithms. AI/ML algorithms can also handle multi-dimensional and multivariate data at high computational speeds. Considering the numerous advantages of AI/ML algorithms, it is easy to understand their exponential and ubiquitous emergence in various fields. With the rapid advancement of VLSI-CAD technology and semiconductor technology, there are ample opportunities in semiconductor and EDA technology to develop AI/ML solutions to automate various processes at various levels

of VLSI design and manufacturing (Koblah et al., 2023; Kumari & Majumder, 2025; Pan et al., 2025).

The EDA tools are mostly old and rules based, and hence make use of shorthand coding languages recognizable uniquely to them to input the design in a suitable format. These rules or coding should be human written and are well documented in the EDA tools' User Manuals. The human coded design and coding languages are often complicated, time consuming, and not so easily abundant and accessible. An ideal EDA tool should overcome the limitations of human commercial VLSI CAD tools in terms of quick, accurate, and optimal outputs—overcoming design constraints effectively. An AI tool should make use of consensus algorithms and programmable design thinking to get universal VLSI CAD (Wang et al., 2024; Yuan et al., 2024).

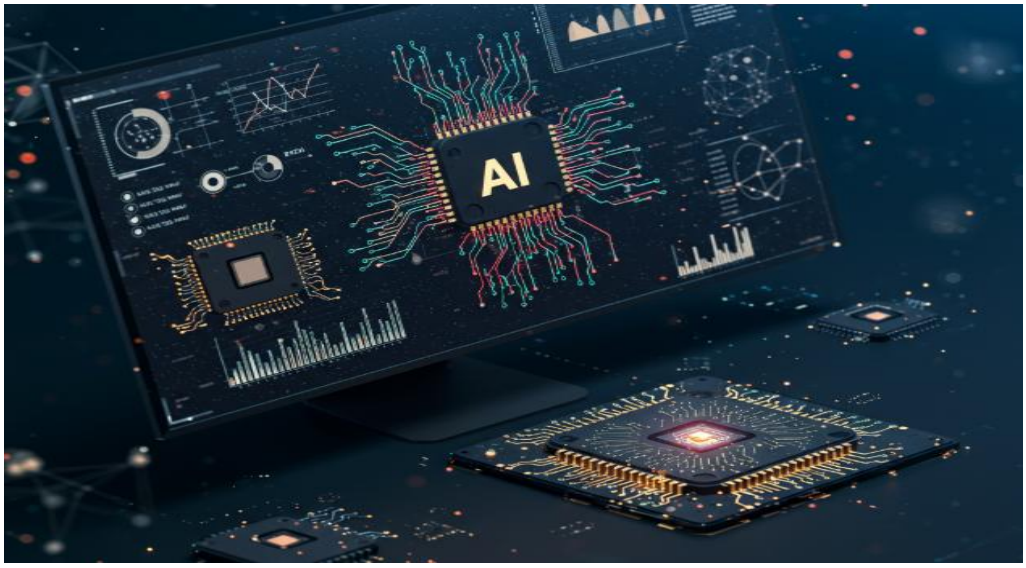

Fig 5.1: AI is Revolutionizing Chip Design

5.1.1. Background and Significance

Electronic design automation (EDA) tools are extensively used to ensure the functional correctness, performance, and manufacturability of large complex integrated circuits (ICs) before fabrication. VLSI circuit designers require quick timing closure of the chip design to reduce the turnaround time (TAT)—the time taken for the IC from the design stage to the final product. There is considerable research expense on the development and enhancement of various EDA tools. However, with a tremendous increase in chips per transistors, it has become increasingly challenging and complex to design ICs

meeting design constraints. New methodologies and tools addressing the challenges and bottlenecks at the various stages in EDA are thus needed.

In more recent technology nodes, with transistor dimensions getting smaller than 20 nm, it is becoming increasingly difficult in terms of fabrication to ensure the desired performance of the synchronous circuits (i.e., circuits with clock edges triggering the operation of latches and flip-flops). Several different process parameters can be varied in fabrication and designated as variabilities. Offsetting this design paradigm shift, spontaneous VLSI technological advancements are being encountered in fabrication processes. Availability of different transistors with different characteristics and flexibility to use them is one alternate design methodology. Multi-gate field-effect transistors (FETs) are more tolerant to process noise, leakage aware, and more advantageous in many other aspects over conventional bulk-type CMOS transistors at nanometer technology nodes. However, in a chip consisting entirely of multi-gate FETs, design integration with traditional CMOS cannot be achieved wholly.

5.2. Overview of Electronic Design Automation

As integrated circuit dimensions shrink, their complexity is increasing exponentially which makes it harder for engineers to design quickly and accurately. The inability to keep up the pace with rapid technological advancement has turned the design process more sophisticated and diverse. This increased complexity has made it infeasible for engineers to design and verify integrated circuits on their own. Thus, architecture design, logic synthesis and circuit implementation, verification and physical design automation has become key components in the overall design flow. The objective of this article is to classify these major circuits/design flows according to EDA tools, architectures and algorithms, and to prepare a balanced overview of applications of all types of artificial intelligence in each category of ten essential design flows. It is also planned to point out the limitations of AI applications, challenging tracks in the near future, and desire capability and intelligence of EDA tools, hence of chips.

Online and on-demand, low cost, rapid turn-around high performance design services will be available. The question of chip architecture will be thrown back to designers because it will always be possible to design a chip that is not manufactureable or testable. All chips should be able to post-silicon test, characterize and fix only with a minimum amount of knowledge about the chip.

5.2.1. History of EDA

IEDA is a collection of powerful and open-source intelligent design and data analysis tools dedicated to the research and development of electronic design automation (EDA) technology. EDA plays an instrumental role in the IC design and fabrication industries, where the rapid increase in chip complexity presents grand challenges for chip designers and EDA developers. A large number of fruitful CAD algorithms, tools, and systems have been developed in academic and industrial circles to tackle critical EDA problems.

The early years of EDA development can be characterized as the "invention and experimentation" era (1960-1975). During this period, the rapid development of integrated circuit (IC) technologies accompanied by the explosion of chip designs and increased complexities raised grand challenges for engineers, resulting in tedious efforts and engineering disasters. It thus became extremely urgent to develop efficacious design automation tools for the IC design house. Designers initially developed tools such as schematic capture, floorplanning, placement, and routing manually. Within a very short period, an extensive number of effective design automation algorithms and tools were invented and developed, which constituted EDA tools as they are conceptualized today.

The computational performance of EDA tools for large-scale problems was low. Industry giants consequently created their own EDA tools, which were often package products with poor connectivity. On the other hand, academia largely worked on the fundamental and theoretical development of EDA tools and algorithms, resulting in many high-quality algorithms with superior performance on benchmark problems. Furthermore, academia was largely isolated from industries and had little influence in the EDA market. In response to these challenges, academia and even small startups endeavored with great enthusiasm to develop their own general-purpose EDA systems.

5.2.2. Key Components of EDA Tools

Electronic Design Automation provides the complete physical design for VLSI circuits. EDA is typically carried out using software containing several components or tools, each performing one or more tasks on the design netlist. As a result, EDA can be thought of as a collection of software tools that produce a single output using some input and follow a specific series of procedures.

Use Case and Limitations: The proposed system is expected to assist the VLSI circuit designer in the design process. First, the designer provides the RTL netlist of the hardware to be designed. The server's AI model produces a complete set of code containing the required EDA tool invocations to perform the desired task with the provided netlist. The long text code can be executed in a Jupyter notebook or terminal with Python. EDA tools in the cloud are to be invoked along with software integration.

Next, the designer inputs synthesized datasets. The data normally contain fifteen decimal values corresponding to one data point. The four decimal points are associated with a specific translator, five with the secondary solver, and six with the main fitter. The AI model, using the provided data, returns a code containing tool invocations of the estimation tools.

Requirements and inputs: The input to the agent call to code assistant consists of a string containing the user's requirements. A REST architecture is used to set up the server. The server runs a large language model that can decode text-to-code for Python language. All EDA tools are independently integrated with APIs that can take files as input and output the result as a PDF or text file. A streaming function is supported to directly view the output from the tools as they produce it.

5.2.3. Current Trends in EDA

Before and after fabrication, input into the physical design flow, AI/ML has been successfully used for runtime and throughput optimization as well as yield prediction and lithography diagnosis optimization. Several tools and architectures based on an AI algorithm or machine learning libraries have been researched for prediction value attainment. Moreover, the prediction ability has been achieved by inputting previous design experience, input-output datasets, or result patterns. AI/ML-based prediction has proven superior to related methods using prior heuristics.

Ample opportunities exist, and a representative example is working with design parameterization knowledge combined with heuristics. Commercial software that captures this knowledge should further investigate its integration into data-based prediction methods. Architectures and tools have been shown at multiple abstraction and hierarchy levels, and efficient fine-tuning and training approaches that guarantee generalizability and transferability have been investigated successfully, thus minimizing the effort required by specialists when using AI/ML.

Commercial software has been developed. However, addressing the ease of deployment into the design flow remains a challenge for AI/ML tools. Research that seamlessly integrates and utilizes AI/ML tools in both academia and industry would allow advancement of the technology in EDA and IC design. Unsurprisingly, a massive amount of funding is heading in this direction, and keeping pace with the availability of data may become a bottleneck.

5.3. Artificial Intelligence: A Primer

Artificial Intelligence (AI) is a branch of the field of computer and information science. It includes both the theory and the practice of developing hardware and software systems equipped with computational components that store, manipulate, and communicate information (data). Thus far, efforts in the field of AI have focused on problem solving. AI research and development efforts have resulted in the good, bad, and ugly of smart tools. AI includes — but is not limited to — such topics as knowledge representation; heuristics; search; expert systems (knowledge-based systems); perception, natural language understanding and production; neural nets; machine learning; robotics; and fuzzy logic systems. Efforts in AI have produced two fundamentally contrasting approaches to solving problems and accomplishing tasks: symbolic (or knowledge-driven) systems and sub-symbolic (or non-knowledge-driven) systems. Symbolic systems include — but are not limited to — expert systems, theorem provers, natural language understanding systems, and certain computer-aided design (CAD) systems. Sub-symbolic systems include — but are not limited to — neural nets, genetic

Fig 5.2: Artificial Intelligence A Primer

algorithms, and simulated annealing. However, it has become increasingly clear that — for many problems/applications — neither of these approaches works well on their own. The field of AI wants to develop machines and software systems that solve problems and accomplish tasks that — if accomplished by humans — would be considered a display of intelligence. The AI field is approximately 50 years old; its roots go back somewhat further, to efforts at problem-solving/puzzle-solving. The traditional approach

to problem-solving is algorithmic or symbolic. It consists of formalizing the problem, stating a solution procedure in a programming language, and executing the solution algorithm. The more sophisticated approach is via heuristics: semi-structured, informal procedures that are not guaranteed to produce a solution but can be viewed as "problem-solving aides." Such richness of content makes AI rather complex, unpredictable, and at times cryptic. AI has had a considerable amount of success in solving certain types of problems. In some cases, these successes are starting to be commercially exploited, albeit in the price range of hundreds of thousands of dollars for consultancy prices.

5.3.1. Definition and Scope

Artificial intelligence (AI) and machine learning (ML) algorithms are playing a prominent role in the electronic design automation (EDA) industry. EDA is an important part of the VLSI chip design flow, aiding designers in rapidly designing complex chips while adhering to corner-case parameters. With advancements in the number of transistors in each technology node, the art of chip design and compliance with design rules has become so intricate that it is impossible for a designer to design a chip manually without using EDA tools, thus resulting in a profitable business for semiconductor foundries and EDA vendors. Semiconductor foundries manufacture chips and supply them to consumers, while EDA software companies sell the software tools which assist a designer in designing a chip.

AI is a wider umbrella term in which a machine performs tasks that normally require human intelligence, such as natural language processing, speech recognition, and computer vision. Machine learning is a subset of AI used when the learning is done by means of data for trend and pattern recognition, while deep learning neural networks perform further deep dives into analyzing complex data. Overall, the goals of AI and ML are learning, reasoning, predicting and perceiving. Overly large chunks of data make it cumbersome for a human to analyze and derive relevant conclusions. AI and ML help overcome this bottleneck. Algorithms identify trends and patterns in vast volumes of data and help users make relevant decisions. This ability to spot trends and associate them with meaningful classes or functions makes their applications endless. AI-ML applications are already vast in consumer products, banking, medical field, manufacturing, real estate, climate research, stock markets, and insurance audits.

5.3.2. Types of AI Technologies

The AI techniques can be broadly classified into the following categories: Machine Learning without Artificial Neural Networks, ML with Artificial Neural Networks,

Computer Vision, and Natural Language Processing. The various algorithms/methods used in each of the classes of AI techniques are listed below in a tabular format.

5.3.3. AI in Engineering Applications

As synthetic intelligence (AI) and enormous records hold to grow, simulation is becoming a commodity. As software becomes more sophisticated and inexpensive, designers are able to simulate large, complex circuits and do layout exploration based on effects. Rapid analysis preamps on a single chip enable the development of fast-sampling multi-channel sampling oscilloscopes for high-frequency measurements. A variety of memory cell structures and array styles has been investigated. A survey of memories available for designers and a prediction of future trends in materials, structures, and parameters were presented. The emphasis is on features and advantages of an integrated approach which considers the entire link from input signals through transmission media to final application, removes the boundary between the IC chip and the printed circuit board enabling reduction in costs and improved performance. With large systems, this approach calls for modeling at a high level. These modeling languages emphasize hierarchical statements close to high-level design. Abstract test generation algorithms and developments in the field of proving the correctness of models against specifications have been outlined. A wide range of packages spanning from academic prototypes to commercial applications have been covered.

Some of these packages are both fully and partially commercialized. Significant improvements over conventional methods have also been reported. Some of these approaches employ relaxation methods to accelerate convergence and handle large systems while others involve algebraic approaches with multigrid acceleration. A unified approach was proposed to obtain filtering structures. Simulation of stray capacitances to wideband circuits was investigated. Also scheming of couplers of novel topologies optimized to conventional technology was undertaken. Finally filters (analog and permanent) were designed with an innovative graphical-oriented package and a new concept of frequency curvature.

5.4. Integrating AI into EDA Workflows

To harness the potential benefits of AI, EDA tools can partially and incrementally incorporate various AI models into their existing workflows. In the context of AI-Assisted EDA Workflows, the Autonomous Scene model divided the workflow into five modules, namely Task Understanding, Knowledge Retrieval, Task Planning, Task Execution, and Result Analysis. Each module contributed to the EDA process from a different perspective, and their effective execution ensured the successful generation of

the final results. AI models can be employed at different fidelity levels, including interfacing with existing ones or being tightly integrated. For domain-specific AI models, circuit designers can record the design iteration of a circuit with underlying hypotheses. The learned engineering knowledge can then be used for redundancy identification to eliminate design errors in future versions. AI models with unrestricted domains can also be utilized in brainstorming novel circuit topology or EDA methods. Overall, after establishing a well-defined integration with human designers, the knowledge base of the EDA tools can be expanded significantly. To enhance an existing AI model's performance in a specific problem, the model can be fine-tuned with corresponding data. Most AI models are trained with publicly available data, and they may not be adept at processing EDA tools, which are inherently domain-specific knowledge. However, by compiling a large knowledge base of EDA tools' usage from publicly available resources, an AI model can be customized to understand the circuits and tools better. It can help interrogate the EDA tools more finely and produce more convincing results. Moreover, through generative techniques, the fine-tuned AI model can help researchers brainstorm new algorithms and even partially generate patents. Together with the seamless interactions between AI models and EDA tools, the design automation of circuitry would thus be further developed.

Various documentation standards exist for different purposes in EDA specifications. Nevertheless, additional standards are often needed for parameter programming compatibility, which can be laborious and complicated. A data source translator might need to be developed for each EDA app. A layered data plan consists of three sections: an information layer, a documentation layer, and a programming layer; and serves as a concise representation for simulation specification. The suggested representation should be independent of any design process and structure to enable input from various tools. Transforming parameters to a limited number of tags reduces initial selection ambiguity by clarifying understanding.

5.4.1. Data Acquisition and Management

Quick access to raw and instrumental data is a pivotal yet daunting task within EDA, as it directly affects the availability and quality of machine learning models. Deciding on the needed data before actual modeling is crucial because limit-induced information loss or damage is very costly. As an inhabiting area of research, many excellent solutions exist; nevertheless, they have rarely been established for an EDA application specifically. Most EDA programs frequently use user- and/or process- specified parameters for simulation. Parameter selection may need to go through up to ten iterations within a large design space of more than hexadecimal traces due to parameter sharing or interdependencies. As a result, a clear and concise representation of use

specifications is essential for all interested parties: designers, modeling specialists, and verification/datasheet engineers. A machine learning representation of knowledge-structure deviation may not be too far-fetched in the next decade.

Among different multi-dimensional visualization styles of data connection extraction, the tanglegram process seems more suitable in EDA as it captures parameter dependency by connecting two trees. The interpretation of document tree pairs is reliant on the sequence of notations. For example, a forest drawing indicates no output affinity of tagged parameters. The input of a forest tree may be represented by parentheses-aligned notation. Searching is another critical task in EDA; a visual query device attached to the process tree helps designers reveal the use intention of any technology. A possible extension of the query method, a way to prompt knowledge displacement, is an active query that addresses the location intention of one or two tree nodes and returns a path for operation.

Governing a machine learning model progressively proves to be a reliable way that is very similar to human learning. To address the inclination of while-stated precision and resulting in out-of-box reasoning, output micro-generating specifies found conditions and randomizes all decision gaps. Producers and users usually might prefer faster, compressed growth; a mental effort output should also be involved in model fatigue estimation, abstraction limitation testing, and local behavior inspection. Various policy stream independence conditions exist for different conditions establishing robot processing sophistication.

5.4.2. AI-Driven Design Automation

Due to aggressive process scaling, shrinking technology nodes, and rising manufacturing costs, electronic design automation (EDA) tool performance is one of the most critical concerns for the semiconductor industry. The complexity of integrated circuits (ICs) is rising exponentially. As a result, the development of quick, efficient, and high-quality EDA tool solutions is required. In addition, fast and efficient designs are required to keep up with market speed and encourage chipmakers to migrate to the next technology node. With advances in IC technology, design complexity continues to rise, leading to increased design automation challenges for design engineers. The primary goal of EDA tools is to ease the design challenges facing design engineers at both the front-end and back-end levels. The turnaround time of a chip depends on the performance of EDA tools in overcoming design constraints.

Nevertheless, such designs often contain very challenging mixed-signal circuit design problems that must adhere to a large number of tightly constrained competing performance specifications. Some designs are so complex that no readily available

human knowledge and design expertise can solve the design problem in a finished design. In such complex cases, the only option is to automate the design of a large portion of the design task. The traditional rule-based methodologies in EDA take longer to yield an optimal solution for the set design constraints. This bottleneck is commonly referred to as "the EDA bottleneck." Though many research papers and ideas gradually make the EDA flow very smooth, there are still many upcoming challenges to be conferred and solved. Additionally, AI-based EDA tools are predicted to become the normative paradigm for the industry within the next ten years. In terms of quantum computing, design for manufacturability (DFM), and AI, EDA tools have the potential to connect with the downstream economic environment. AI has provided prominent solutions to many problems in various fields such as healthcare, finance, management, and many more vertical segments.

Artificial intelligence (AI) is the provision of human-like intelligence to non-human entities or computers. Deploying algorithms, machines, and software to think and act like humans is broadly termed AI. AI can also refer to creating systems that can act in a self-learning and pre-programmed manner to solve problems. Machine learning (ML) is a subset of AI, which is also the application of AI. The goals of AI/ML explicitly relate to learning, reasoning, predicting, and perceiving. AI/ML can quickly identify the trends and patterns in large volumes of data, enabling users to make relevant decisions. AI/ML algorithms can handle multi-dimensional and multivariate data at high computational speeds. Considering the numerous advantages of AI/ML algorithms, their applications are endless.

VLSI–computer-aided design (CAD) tools are involved in several stages of chip design flow. Out of these stages, the design and performance evaluation of highly complex digital and analog ICs depends on the CAD tools' capability. Advancement of VLSI–CAD tools is becoming increasingly challenging and complex with the tremendous increase in transistors per chip. The design activity will occupy the largest share of the entire chip design time as technology scaling continues. As a result, several opportunities are available in semiconductor and EDA technology for developing/incorporating AI/ML solutions to automate processes at various VLSI design and manufacturing levels. The primary work done in this paper is to present the application of AI/ML algorithms on topics in VLSI CAD and design automation that are popular, impactful and have significant potential for use of AI/ML algorithms.

The scope of discussion includes the application of Convolutional Neural Networks (CNNs) and other deep learning (DL) algorithms for CAD problems like layout extraction, circuit netlist generation, signal integrity analysis, etc. Reinforcement learning algorithms for the design of domain-specific algorithms in CAD tools for physical design automation are discussed. AI/ML-based advance timing optimization using multi-corner and multi-mode static timing analysis with a selection of optimization

algorithms is discussed. Local pattern matching embeddings and circuit characterization of standard cell libraries using instance-specific linear regression algorithms are discussed. AI/ML-based systematic analog circuit design automation for popular blocks like biasing circuits, current mirrors, voltage references, operational amplifiers, etc. using supervised, reinforcement, and generative modeling approaches are discussed.

5.4.3. Machine Learning for Circuit Design

The applications of machine learning in Electronic Design Automation (EDA) range from Machine Learning (ML) based designs, where ML algorithms are used in designing either software or hardware functionality, to using ML to assist with EDA problems encountered during physical design. Therefore, a typical ML flow consists of: (i) Data preparation and transformation, where data is either simulated or extracted from a given champion data. At this stage, data can be transformed to other formats if necessary; (ii) Model selection, where the architecture that substitutes the given EDA task is selected. It can involve using simple ML models or implementing deep networks with several experimental runs; (iii) Model training and evaluation, where relevant metrics are defined based on how the model is fit to the simulated/truth labels, along with real production data constraint checks. It usually involves either supervised or unsupervised learning and/or Hyper-parameter tuning; (iv) Model deployment, where the models are incorporated in EDA tool flow, either in an offline mode or in the loop with on-chip optimization.

Such pathways are applicable for a variety of EDA tasks, including those dealing with simulation data, graph-like data, string-like data, and {mixed, unlikely combinations}. It is complex and ambiguous to categorize EDA tasks in the aforementioned definitions, so the focus is on tackling specific EDA tasks rather than on database formation. In this survey, the ML approaches for different EDA tasks like cell placement, timing optimization, post layout design-rule-check, and pointer netlist generation are described. Classic methods with state of the art ML algorithms are addressed in detail as success stories, along with discussions of pros and cons.

The Digital VLSI design flow consists of several important steps: RTL design, synthesis, place & route (P&R), DRC, extraction, and circuit simulation. In each step, unique problems must be solved while fulfilling a series of constraints, including timing closure, technology rules, power & performance, yield, etc. Some of these problems can be efficiently solved using hard-coded algorithms/heuristics and are in few core commercial tools. However, several problems remain difficult due to their computational complexity or lack of thorough problem formulations. A majority of these yet-unresolved problems are tackled using custom EDA flows with human experts involved to fulfill requirements. With technology advancement on both the design and manufacturing side,

a growing dataset and potential knowledge are available in the form of both simulated and production data extraction.

5.5. Benefits of AI in Chip Design

The gradual involvement of AI in each phase of IC design is beneficial for designers, engineers, and the overall EDA, besides reducing the design cycle time. The arrival of AI is expected to tackle the current challenges of crowded design specifications and exploding costs of design and process development, fabrication, and testing in chip design [1]. Artificial & Machine Learning (AML) methods have been introduced, and tools developed to take advantage of analytical and statistical methods for various tasks in system design and verification, physical design, timing verification, testing, etc. The transformed methodologies are more scalable than original ones, enabling the addressing of problems at a much higher complexity. A more profound impact is expected from the acceleration of AMD and general implementation of neural networks by GPU/FPGA/ASIC hardware accelerators through recent advances in neural architecture, representation learning, the availability of big data, etc. The EDA algorithms based on these new architectures, paradigms, and workflows would not only be more scalable but also fundamentally different from the traditional methods. Nevertheless, there are issues to be resolved to create reliable EDA tools with AI at each stage of chip design and tackle its grand challenges sparked by new deep-learning techniques.

Fig : Innovative Is China in Semiconductors

Demand for AI chips is growing exponentially due to continuously growing data generation and its associated analytics in various sectors. This demand for performance, power, and area is extremely tough and the existing chips need to be fashioned again with radical architectural changes. This poses challenges on architecture research since existing principles of them are impossible to follow. The ever-going global tech war is creating trade->war tech barriers, which leads to abrupt growth of local portrait foundries or unexpected bankruptcy to establish some other advanced nodes by existing foundries. This significantly increases the design complexity on unseen technologies due to an uncontactable process corner. As semiconductor technology nodes become smaller, the side effects of their inherent physics increase. It results in variability in both functional and physical domains - to databook and exhibiting a power law behavior.

5.5.1. Increased Efficiency

Electronic design automation (EDA) is a key area in computer-aided design (CAD) and is crucial for the development of digital systems. The exponential growth of design complexity has resulted in the widespread usage of automatic algorithms. EDA has advanced significantly in the past 40 years. During the earlier eras of EDA, heuristic algorithms were defined explicitly and were problem-specific. Around the end of the 1990s, with the growth of computer processing speed, more generic and broader algorithms came into focus, targeting various applications. A sufficient amount of library data was then available for better initialization of the algorithms, which increased their convergence speed. This in effect broadened the applications of meta-heuristics in industrial CAD tools for timing closure and physical design. Even in the last decade, the industry has witnessed a dramatic increase in capacity, which amplified the scale and complexity of backend designs. More importantly, advanced technology nodes have also been adopted for AI, which brought more challenges to the design aspects in both processing and manufacturing. The capacity limit of computers has also been challenged, which resulted in updated versions of older EDA algorithms. In this background, academia embraces more autonomy from the industry regarding numerical algorithms, which has resulted in a wealth of algorithms, software and ideas that can be revisited for new potential. Many emerging techniques in optimization, classification, modeling, simulation, etc. can be well adapted in EDA applications and are expected to have huge potentials, because they have different convergence speeds, accuracy ranges and solution accuracies. In this context, machine learning (ML), especially deep learning (DL), has attracted extensive attention and has been adopted in many fields. However, its applications in EDA are still limited. Thus, the goal of this review is to summarize existing ML-based methods for various applications in EDA. The specific objectives are as follows: 1) identify the necessity of applying ML in EDA; 2) review existing ML-based methods for diverse EDA tasks; 3) delineate the challenges of this riveting area

for future research directions in more depth; and 4) point out the challenges and open issues in detail.

5.5.2. Enhanced Accuracy

With the increasing economic demands, many ASIC/FPGA designs are pushed to several hundred million gates, resulting in an ever-growing optimization resource consumption and hindering users from achieving the desired quality of results in time. Many advanced EDA tools are adopting AI-based methods to accelerate analysis and optimization, resulting in significant speedup compared to traditional computational methods. Early AI-based VLSI design systems performed layout generation/trimming, placement, and routing. After this, they were proposed for netlist synthesis, estimation and fault detection of manufacturing defect, and circuit simulation. The use of AI algorithms and heuristics in EDA tools is certainly not new. Hence, after a comprehensive introduction to EDA, basic definitions and parameters, corresponding AI/ML models and algorithms are provided along with practical examples on their use in EDA tools.

Recently, many AI approaches have been used for 2D FE-based post-layout RC extraction. A two-step method is developed to obtain accurate and efficient parasitic capacitance extraction results based on a combination of ML and the FEM, which has been incorporated into Synopsys StarRC. A fast post-layout 3D RC extraction flow using the AI approach is also reported, which includes two phases of a machine-learning-enabled SRAMs RC extraction flow. Post-processing was conducted on the extracted RC nets to achieve speedup of various timing analysis tasks.

The rapid advancements in electronic products and technology have put tremendous pressure on the semiconductor industry. Semiconductor devices are continuously integrated into smaller areas, consuming reduced power and yet achieving higher performance at a lower price. For example, the number of transistors on an integrated circuit (IC) is estimated to double in size every 18 months, according to Moore's law. However, this new generation technology is getting very complicated. In particular, with the introduction of multi-patterning, with reduced technology nodes, the number of possible design rules has taken a huge leap. The industry has come to realize that new computational approaches are required in solving these complicated problems and satisfying these new design rules.

On the one hand, there has been a ton of new research in different advanced forms of computing, including approximate computing, CPU-GPU collaboration, etc. These forms of computing take advantage of huge performance gains provided by new hardware architectures. Implementing well-studied algorithms into these new forms of

computing could gain performance improvements over standard computing platforms greatly. On the other hand, with the growing availability of very large datasets and dramatic advances in machine learning, there has also been a surge of interest in using learning algorithms as alternative computational engines to design chips, detect faults, and even predict future VLSI designs.

5.5.3. Cost Reduction

primary driving force for the down-scaling process. Over the years, the dimensions of the logic devices have shrunk at a maximum rate of Moore's law and became smaller than the resolvable feature size and the working function of the semiconductor technology. Such continued shrinkage has brought about new challenges in manufacturing a chip, especially the interconnectivity among the devices. The level of manufacturing process complexity has attained an avalanche increase resulting in huge fabrication costs. Current technology nodes fabricated in weak lithography are generally considered the corner process technology nodes. The level of design complexity has also increased at an unmanageable level in pentascale designs. As a stewardship on design productivity, the advancing of design tools is the key to the declivity region of the Kumar curve below 280 nm. In other words, there is no tactical retreat for existing design tools since otherwise, design productivity will be exponentially deteriorated. The complexity of design tools is also expected to increase proportionately. In contrast to the other areas of CAD research that are currently processing at a static state, the dynamic nature of AI learning methods could be two-phased of inherent cracks for the other than standard CAD methods.

Conventionally, a large number of methodologies have been developed for the CAD of VLSI chips on a cost and time-effective basis. High demands, various potentials and prospects, investments, and research-collaborations have been devoted and pursued. Nevertheless, no one architecture of these CAD tools has yet been matured and established as a standard flow of usage, preventing their practical applications in a wider community. Machine learning (ML) and AI learning algorithms have been investigated and proposed for a wide range of learning strategies and tasked problems. In terms of their wide availability, easy engineering, and relatively low requirements of the training database, these learning algorithms are anticipated to unfold their usage on a variety of VLSI CAD methods, especially on the methodology development and optimization of cost and time-effective basis. More generally, learned tools can be of network architectures facilitating parallel computation in a workstation with variable computing cores.

5.6. Conclusion

Artificial intelligence (AI) and machine learning (ML) algorithms are playing an increasingly critical role in the electronic design automation (EDA) of silicon devices. Given the challenges posed by modern nanometer-scale semiconductor technologies, the need for EDA techniques that are faster, smarter, and more reliable has never been more critical. AI, with its versatility and flexibility, is well-suited to this task. In contrast to conventional techniques that leverage rule-based methodologies, AI/ML techniques have access to a wealth of historical data as well as other design and technology-specific data that were previously considered untouchable. By rapidly identifying trends and patterns in the data, AI/ML techniques can create smart heuristics to automate the design process and quickly overcome a host of design constraints. This is true across many aspects of the semiconductor design ecosystem, from modeling to academic and industrial design practices. In particular, in VLSI design and EDA technology, many new opportunities are opening up for the development and incorporation of AI/ML solutions that will allow the automation of hitherto manual processes.

Narrowing down to the current capabilities of AI and ML, the challenges and requirements necessary for tackling the application of state-of-the-art AI to EDA/modeling are discussed. The findings highlight a sizable gap between the capabilities of existing AI/ML solutions and the design automation needs in the semiconductor ecosystem. AI/ML algorithms for VLSI design and modeling at various abstraction levels are extensively summarized, and the literature reviewed from circuit-level to system-level design automation. The opportunity areas to benefit from AI/ML at each of the design phases are discussed, as well as the possible AI/ML approaches that can benefit from existing solutions in the broader world.

5.6.1. Future Trends

The maturity of machine learning (ML) tools, increased investment in ML research and development by leading semiconductor companies and academia, and the growing awareness of ML techniques' usefulness to solve EDA problems are expected to aid the adoption and deployment of ML techniques to address traditional and emerging EDA challenges. A broad scope view of ML in EDA reported more than 1,000 applications in CAD and analysis flows. Applications by categories include EDA-related tasks at various levels of design abstraction, techniques selected by applications, and the resources leveraged to train the models.

With the consent and collaboration of semiconductor companies and expert researchers, this survey endeavored to remove obstacles for newcomers to ML in EDA and spread awareness of opportunities to explore new applications for existing research

communities. Newcomers can find success stories of ML applications in EDA reported in journals, guidance on suitability matched methods of machine learning techniques to EDA tasks, and EDA-oriented design environments as sandbox resources for the implementation of ML tools. The growing interest of the EDA and IC design-related industry in deploying ML tools bodes well for the expansion of the toolkit offered by researchers and their commercial implementation. International ML in EDA events are expected to be launched in support of this expansion.

The resurgence of ML techniques has made a profound impact across all disciplines, including electronic design automation (EDA). The wide-spread adoption of these techniques by EDA companies to solve scattered problems and by semiconductor companies to leverage the plethora of EDA data through the collaboration with EDA companies and the involvement of academic institutions have further accelerated their impact. These proposed tasks and expected trends are expected to guide researchers to narrow the search space with respect to the potentially impactful research directions, and motivate EDA companies and researchers to fill in the gaps and provide new directions to explore under-addressed and completely uninformed problems.

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